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COMMITTEE LETTER BALLOT
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SUBJECT: LPDDR4 Spec.

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Features

- Ultra-low-voltage core and I/O power supplies
- V_{DD1} = 1.70–1.95V: 1.8V nominal
- V_{DD2}/V_{DDQ} = 1.06–1.17V: 1.10V nominal
- 4Gb–32Gb
- x16 data interface
- 2-channel partitioned architecture for low read/write energy and low average latency

Up to 17 GB/s per die (2-chan x 8.5GB/s)

- Data rates up to 4.26 Gb/s per pin
- Small page size for low activate energy
- 16*n* prefetch per channel for high-bandwidth performance
- 8 internal banks per channel
- Single data rate CMD/ADR entry
- Bidirectional data strobe (DQS) per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths: BL = 16, 32
- Low-swing, single-ended, V_{SSQ}-terminated I/O
- V_{OH}-compensated output drive I/O
- Programmable V_{SSQ} (ODT) termination
- On-chip temperature sensor to control self refresh rate
- Directed per-bank refresh for concurrent bank operation
- Partial array self refresh (PASR)
- Clock-stop capability
- Programmable CA_ODT and DQ_ODT with V_{ss} termination

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency (Set "A")	WRITE Latency (Set "B")	READ Latency (No DBI)	READ Latency (With DBI)
-046	2133	4267	18	34	36	40
-053	1866	3733	16	30	32	36
-062	1600	3200	14	26	28	32
-075	1333	2667	12	22	24	28
-093	1066	2133	10	18	20	22
-125	800	1600	8	12	14	16
-187	533	1066	6	8	10	12
-375	266	533	4	4	6	6

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General Description

The 4–32Gb Mobile Low-Power DDR4 SDRAM (LPDDR4) devices are high-speed CMOS, dynamic random-access memories. Emphasis is on energy per bit savings in both the memory core and the I/O. A small page size (2KB) reduces the activation energy (I_{DD0}), which consumes up to 30% of the device power budget in multicore, multithread systems. A 2-channel architecture reduces the average round-trip latency as seen from the controller, while shortening data routing in the core and reducing read and write energy (I_{DD4}). A low-swing, V_{SSQ}-terminated I/O with data bus inversion is implemented to reduce I/O energy per bit and improve signal integrity. LPDDR4 supports 4–32Gb and is capable of delivering 17 GB/s of total bandwidth per die.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t and DQS_c, and CK_t and CK_c, respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Functional Description

Micron's Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory. The device is internally configured with 2 x16 channels and 8 banks per channel.

LPDDR4 uses a 2-tick, single-data-rate (SDR) protocol on the CA bus to reduce the number of input signals in the system. The term "2-tick" means that the command/address is decoded across two transactions, such that half of the command/address is captured with each of two consecutive rising edges of CK. The 6-bit CA bus contains command, address, and bank information. Some commands such as READ, WRITE, MASKED WRITE, and ACTIVATE require two consecutive 2-tick SDR commands to complete the instruction.

LPDDR4 uses a double-data-rate (DDR) protocol on the DQ bus to achieve high-speed operation. The DDR interface transfers two data bits to each DQ lane in one clock cycle and is matched to a 16*n*-prefetch DRAM architecture. A write/read access consists of a single 16*n*-bit-wide data transfer to/from the DRAM core and 16 corresponding *n*-bit-wide data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected column address and continue for a programmed number of columns in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command to open a row in the memory core, followed by a WRITE or READ command to access column data within the open row. The address and bank address (BA) bits registered by the ACTIVATE command are used to select the bank and row to be opened. The address and BA bits registered with the WRITE or READ command are used to select the bank and the starting column address for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. Following sections provide detailed information about device initialization, register definition, command descriptions and device operations.

Figure 1: Functional Block Diagram

Placeholder

SDRAM Addressing

Where applicable, a distinction is made between per-channel and per-die parameters. All bank, row, and column addresses are shown per-channel.

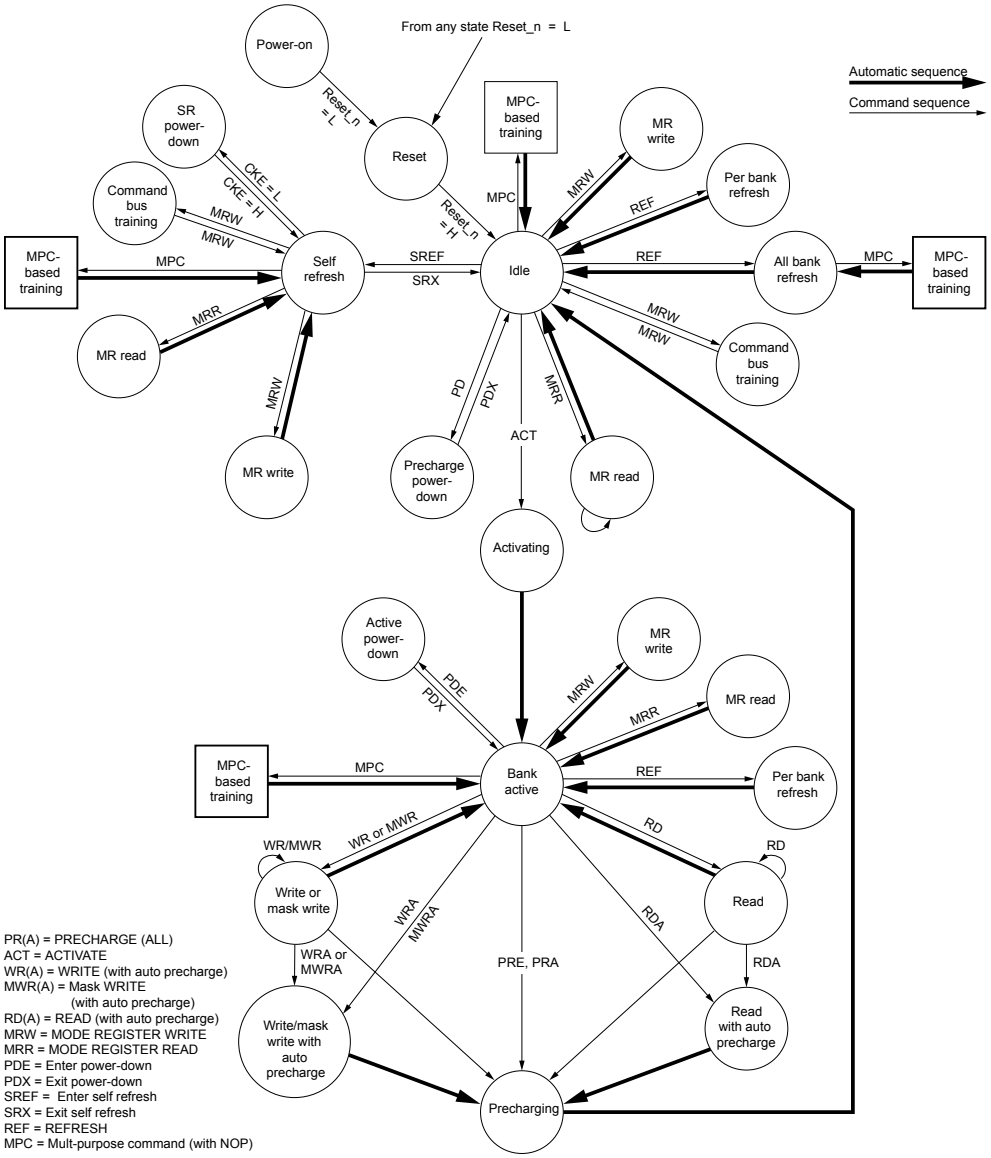
Device density (per die)		4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Device density (per channel)		**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**
Configuration		16Mb x 16 DQ x 8 banks x 2 channels	24Mb x 16 DQ x 8 banks x 2 channels	32Mb x 16 DQ x 8 banks x 2 channels	48Mb x 16 DQ x 8 banks x 2 channels	64Mb x 16 DQ x 8 banks x 2 channels	TBD x 16 DQ x TBD banks x 2 channels	TBD x 16 DQ x TBD banks x 2 channels
Number of channels (per die)		2	2	2	2	2	2	2
Number of banks (per channel)		8	8	8	8	8	TBD	TBD
Array prefetch (bits)		256	256	256	256	256	256	256
Number of rows (per bank)		16,384	24,576	32,768	49,152	65,536	TBD	TBD
Number of columns (fetch boundaries)		64	64	64	64	64	TBD	TBD
Page size (bytes)		2048	2048	2048	2048	2048	TBD	TBD
Channel density (bits per channel)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total density (bits per die)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank address		BA0–BA2	BA0–BA2	BA0–BA2	BA0–BA2	BA0–BA2	TBD	TBD
x16	Row addresses	R0–R13	R0–R14 (R13 = 0 when R14 = 1)	R0–R14	R0–R15 (R14 = 0 when R15 = 1)	R0–R15	TBD	TBD
	Column addresses	C0–C9	C0–C9	C0–C9	C0–C9	C0–C9	TBD	TBD
Burst starting address boundary		64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit

Notes:
1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."
3. For non-binary device densities, only half of the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.

Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

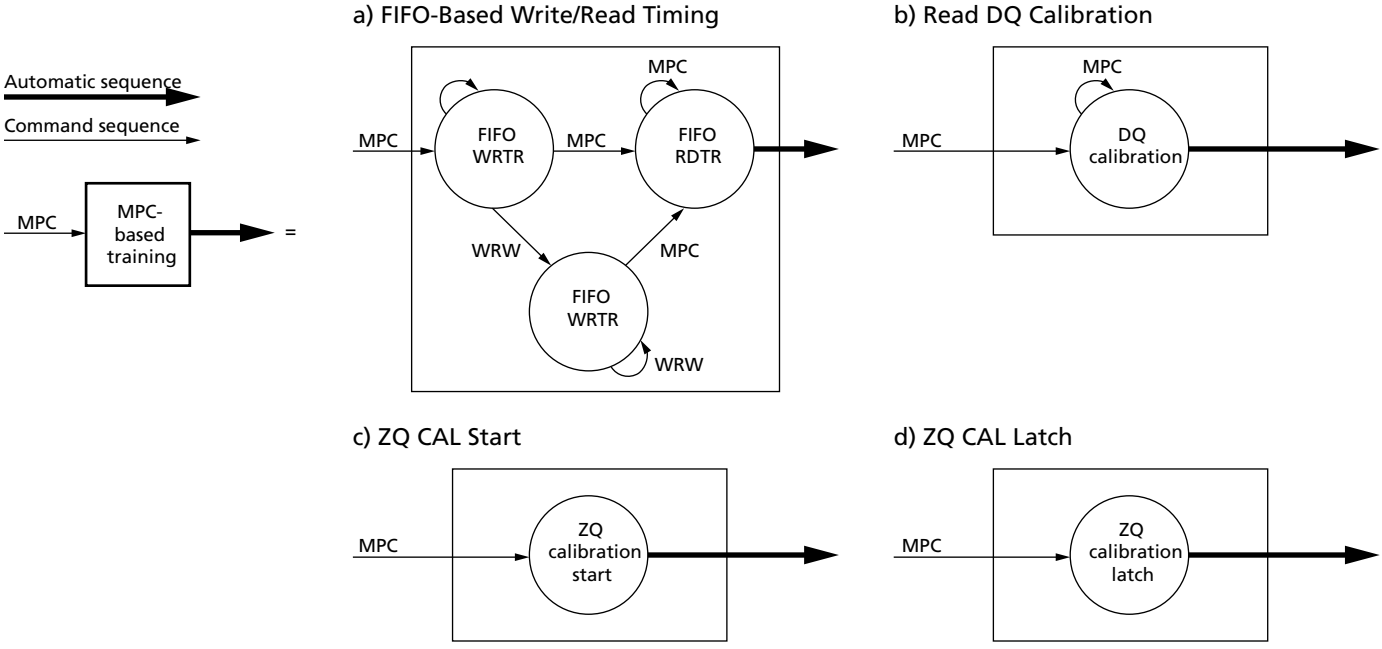
Figure 2: Simplified State Diagram



Notes:
1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are precharged in the idle state.

3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

Figure 3: Simplified State Diagram



Notes:
1. From the self refresh state, the device can enter power-down, MRR, MRW, or MPC states. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.

4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on state as an example, but this should not be construed as a restriction on RESET.

Bond Pad Arrangement

The die connections to the package substrate will be made via wire bonds. Pads on Channel A should be mirrored across the vertical axis to Channel B.

Figure 4: LPDDR4 Pad Sequence

Channel A Top		Channel A Bottom		Channel B Top		Channel B Bottom	
1	V_{DD2}	41	V_{DD2}	1	V_{DD2}	41	V_{DD2}
2	V_{SS}	42	CKE	2	V_{SS}	42	CKE
3	V_{DD1}	43	CS	3	V_{DD1}	43	CS
4	V_{DD2}	44	V_{SS}	4	V_{DD2}	44	V_{SS}
5	V_{SS}	45	CA1	5	V_{SS}	45	CA1
6	V_{SSQ}	46	CA0	6	V_{SSQ}	46	CA0
7	DQ8	47	V_{DD2}	7	DQ8	47	V_{DD2}
8	V_{DDQ}	48	ODT_CA	8	V_{DDQ}	48	ODT_CA
9	DQ9	49	V_{SS}	9	DQ9	49	V_{SS}
10	V_{SSQ}	50	V_{DD1}	10	V_{SSQ}	50	V_{DD1}
11	DQ10	51	V_{SSQ}	11	DQ10	51	V_{SSQ}
12	V_{DDQ}	52	DQ7	12	V_{DDQ}	52	DQ7
13	DQ11	53	V_{DDQ}	13	DQ11	53	V_{DDQ}
14	V_{SSQ}	54	DQ6	14	V_{SSQ}	54	DQ6
15	DQS1_t	55	V_{SSQ}	15	DQS1_t	55	V_{SSQ}
16	DQS1_C	56	DQ5	16	DQS1_c	56	DQ5
17	V_{DDQ}	57	V_{DDQ}	17	V_{DDQ}	57	V_{DDQ}
18	DMI1	58	DQ4	18	DMI1	58	DQ4
19	V_{SSQ}	59	V_{SSQ}	19	V_{SSQ}	59	V_{SSQ}
20	DQ12	60	DMI0	20	DQ12	60	DMI0
21	V_{DDQ}	61	V_{DDQ}	21	V_{DDQ}	61	V_{DDQ}
22	DQ13	62	DQS0_c	22	DQ13	62	DQS0_c
23	V_{SSQ}	63	DQS0_t	23	V_{SSQ}	63	DQS0_t
24	DQ14	64	V_{SSQ}	24	DQ14	64	V_{SSQ}
25	V_{DDQ}	65	DQ3	25	V_{DDQ}	65	DQ3
26	DQ15	66	V_{DDQ}	26	DQ15	66	V_{DDQ}
27	V_{SSQ}	67	DQ2	27	V_{SSQ}	67	DQ2
28	ZQ	68	V_{SSQ}	28	RESET_n	68	V_{SSQ}
29	V_{DDQ}	69	DQ1	29	V_{DDQ}	69	DQ1
30	V_{DD2}	70	V_{DDQ}	30	V_{DD2}	70	V_{DDQ}
31	V_{DD1}	71	DQ0	31	V_{DD1}	71	DQ0
32	V_{SS}	72	V_{SSQ}	32	V_{SS}	72	V_{SSQ}
33	CA5	73	V_{SS}	33	CA5	73	V_{SS}
34	CA4	74	V_{DD2}	34	CA4	74	V_{DD2}
35	V_{DD2}	75	V_{DD1}	35	V_{DD2}	75	V_{DD1}
36	CA3	76	V_{SS}	36	CA3	76	V_{SS}
37	CA2	77	V_{DD2}	37	CA2	77	V_{DD2}
38	V_{SS}			38	V_{SS}		
39	CK_c			39	CK_c		
40	CK_t			40	CK_t		

Channel A Channel B Supply Ground

Ball Descriptions

Table 2: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_tand CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. AC timings for CA parameters are referenced to CK. Each channel (A and B) has its own clock pair.
CKE_A, CKE_B	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. Each channel has its own CKE signal.
CS_A, CS_B	Input	**Chip select:** Considered part of the command code. Each channel has its own CS signal
CA[5:0]_A, CA[5:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	**CA ODT control:** Used in conjunction with the mode register to turn on/off the on-die-termination for CA pins. It is bonded to V_{DD2} within the package or at the package ball for the terminating rank, and the nonterminating ranks are bonded to V_{SS} (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM rank that terminates the CA bus for all die on the same channel.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets both channels of the die.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A , DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Read strobe:** DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The read strobe is generated by the DRAM for a READ and is edge-aligned with data. The read strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a read strobe signal pair. Each channel has its own DQS strobes.
DBI[1:0]_A, DBI[1:0]_B	I/O	**Data bus inversion:** A bidirectional signal which is driven HIGH when the data on the data bus is inverted or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. Each byte of data has a DBI signal. Each channel has its own DBI signals.
ZQ	Reference	**Calibration reference:** Used to calibrate the output drive strength and termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V_{DDQ} through a 240Ω, ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Gnd	**Ground reference:** Power supply ground reference.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Power-Up and Initialization

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.

Table 3: Mode Register Default Settings

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FP-OP/WR[0] are enabled
WLS	MR2 OP6	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
*n*WR	MR1 OP[6:4]	000b	*n*WR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA_ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
$V_{REF(CA)}$ setting	MR12 OP[6]	1b	$V_{REF(CA)}$ range[1] is enabled
$V_{REF(CA)}$ value	MR12 OP[5:0]	001101b	Range1: 27.2% of V_{DDQ}
$V_{REF(DQ)}$ setting	MR14 OP[6]	1b	$V_{REF(DQ)}$ range[1] enabled
$V_{REF(DQ)}$ value	MR14 OP[5:0]	001101b	Range1: 27.2% of V_{DDQ}

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Voltage Ramp

1. While applying power (after Ta), RESET_n should be held LOW ($\leq 0.2 \times V_{DD2}$), and all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

Table 4: Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	$V_{DDQ} \leq V_{DD2} \leq V_{DDQ}+200mV$

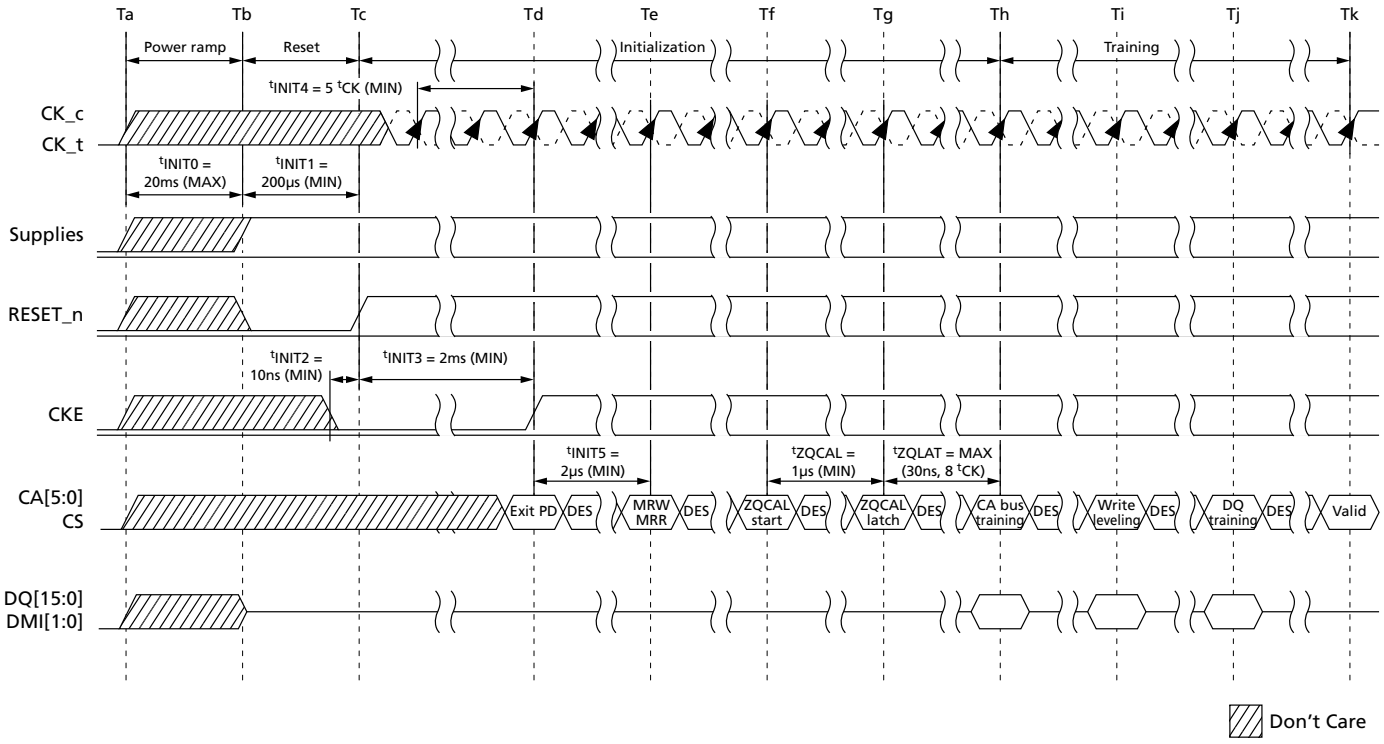
Notes:
1. Ta is the point when any power supply first reaches 300mV.
2. Noted conditions apply between Ta and power-down (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration $^{t}INIT0$ (Tb – Ta) must not exceed 20ms.
5. The voltage difference between any V_{SS} and V_{SSQ} must not exceed 100mV.

2. Following completion of the of the voltage ramp (Tb), RESET_n must be held LOW for $^{t}INIT1$. DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be

between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table below.

3. Beginning at Tb, RESET_n must remain LOW for at least ^{t}INIT1, after which RESET_n can be de-asserted to HIGH. CKE must be set LOW at least 10ns before RESET_n de-assertion. All other input signals are "Don't Care."

Figure 5: Voltage Ramp and Initialization Sequence



Note: 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

4. After RESET_n is de-asserted, wait at least ^{t}INIT3 before activating CKE. CK_t, CK_c must be started and stabilized for ^{t}INIT4 before CKE goes active. CS must remain LOW when the controller activates CKE.

5. After CKE is set to HIGH, wait a minimum of ^{t}INIT5 to issue any MRR or MRW commands. For MRR and MRW commands, the clock frequency must be within the range defined for ^{t}CKb. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the pull-up, pull-down, and Rx termination values, the controller can issue the ZQCAL START command to the memory. This command is used to calibrate the V_{OH} level and the output impedance over process, voltage, and temperature. In systems where more than one device share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each device. The ZQ calibration sequence is completed after ^{t}ZQCAL (Tg). The ZQCAL LATCH command must be issued to update the DQ drivers and DQ + CA ODT to the calibrated values.

7. After ^{t}ZQLAT is satisfied (Th), the command bus (internal $V_{REF(CA)}$, CS, and CA) should be trained for high-speed operation by issuing an MRW command (command bus training mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The device will power-up with receivers configured for low-speed operations and with $V_{REF(CA)}$ set to a default factory setting. Normal device operation at clock speeds higher than ^{t}CKb may not be possible until command bus training is complete. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and it outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, the controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is HIGH and CKE is LOW. See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the controller adjusts write DQS_t/_c timing to the point where the device recognizes the start of write DQ data burst with desired WRITE latency.

9. After write leveling, the DQ bus (internal $V_{REF(DQ)}$, DQS, and DQ) should be trained for high-speed operation using the MPC TRAINING commands and by issuing MRW commands to adjust $V_{REF(DQ)}$. The device will power-up with receivers configured for low-speed operations and with $V_{REF(DQ)}$) set to a default factory setting. Normal device operation at clock speeds higher than ^{t}CKb should not be attempted until DQ bus training is complete. The MPC READ CALIBRATION command is used together with MPC FIFO WRITE/READ commands to train the DQ bus without disturbing the memory array contents. See the DQ Bus Training section for more information on the DQ bus training sequence.

10. At Tk, the device is ready for normal operation and is ready to accept any valid command. Any mode registers that have not previously been configured for normal operation should be written at this time.

Table 5: Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
^{t}INIT0	–	20	ms	Maximum voltage ramp time
^{t}INIT1	200	–	µs	Minimum RESET_n LOW time after completion of voltage ramp
^{t}INIT2	10	–	ns	Minimum CKE LOW time before RESET_n goes HIGH
^{t}INIT3	2	–	ms	Minimum CKE LOW time after RESET_n goes HIGH
^{t}INIT4	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
^{t}INIT5	2	–	µs	Minimum idle time before first MRW/MRR command
^{t}ZQCAL	1	–	µs	ZQ calibration time
^{t}ZQLAT	max 30ns (8 ^{t}CK)	–	ns	ZQ latch quiet time
^{t}CKb[1]	TBD	TBD	ns	Clock cycle time during boot

Note: 1. The controller must guarantee operation at the boot frequency.

Reset Initialization With Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x V_{DD2} anytime reset is needed. Maintain RESET_n for a minimum of ^{t}PW_RESET. CKE must be pulled LOW at least 10ns before de-asserting RESET_n.
2. Repeat steps 3–10 of the Power-Up and Initialization sequence.

Power-Off Sequence

Controlled Power-Off

While powering off, CKE must be held LOW (≤0.2 x V_{DD2}); all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while CKE is held LOW.

DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK_t, CK_c, CS, and CA input levels must be between V_{SS} and V_{DD2} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the minimum DC Operating Condition.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 6: Power Supply Conditions

The voltage difference between V_{SS} and V_{SSQ} must not exceed 100mV.

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	$V_{DDQ} \le V_{DD2} \le V_{DDQ}$ + 200mV

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met.

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 7: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Power-off ramp time	^{t}POFF	–	2	sec

Mode Registers

Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 8: Mode Register Assignments

Notes 1–5 apply to entire table

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	CATR	RFU	RFU	RZQI		RFU			Go to MR0
1	01h	Device feature 1	W	PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL		Go to MR1
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL			Go to MR2
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			WR PST		PU-Cal	Go to MR3
4	04h	Refresh and training	R /W	TUF	RFU		PPRE	RFU	Refresh rate			Go to MR4
5	05h	Basic config-1	R	LPDDR4 Manufacturer ID								Go to MR5
6	06h	Basic config-2	R	Revision ID1								Go to MR6
7	07h	Basic config-3	R	Revision ID2								Go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		Go to MR8
9	09h	Test mode	W	Vendor-specific test mode								Go to MR9
10	0Ah	I/O calibration	W	Calibration code							ZQ RST	Go to MR10
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT			Go to MR11
12	0Ch	$V_{REF(CA)}$	R/W	RFU	VR-CA	$V_{REF(CA)}$						Go to MR12
13	0Dh	Register Control	R/W	FSP-OP	FSP-WR	DME	RFU	VRCG	VRO	RFU	CBT	Go to MR13
14	0Eh	$V_{REF(DQ)}$	R/W	RFU	VR-DQ	$V_{REF(DQ)}$						Go to MR14
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration								GO to MR15
16	10h	PASR_Bank	W	PASR bank mask								Go to MR16
17	11h	PASR_Seg	W	PASR segment mask								Go to MR17
18	12h	IT-LSB	R	DQS Oscillator –LSB								Go to MR18
19	13h	IT-MSB	R	DQS Oscillator – MSB								Go to MR19
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration								Go to MR20
21	15h	Vendor Use	W	Vendor Specific Mode Register								Go to MR21
22	16h	ODT feature 2	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SoC ODT			Go to MR22
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting								Go to MR23

Table 8: Mode Register Assignments (Continued)

Notes 1–5 apply to entire table

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
24	18h	TRR control	R/W	TRR enable	TRR bank address			Unltd MAC	MAC value			Go to MR24
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0	Go to MR25
26–31	1Ah~1Fh	–	–	Reserved for Future Use								
32	20h	DQ calibration pattern A	R	See DQ Calibration section								Go to MR32
33–39	21h≈27h	Do not use	–	Do Not Use								
40	28h	DQ calibration pattern B	R	See DQ Calibration section								Go to MR40
41–47	29h≈2Fh	Do not use	–	Do Not Use								
48–63	30h≈3Fh	Reserved	–	Reserved for Future Use								

Notes:
1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.

MR0:1

Table 9: MR0 Device Feature 0 (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CATR	RFU		RZQI		RFU		

Table 10: MR0 Op-Code Bit Definitions

Register Information	Tag	Type	OP	Definition	Notes
Built-in self-test for RZQ information	RZQI	Read only	OP[4:3]	00b: RZQ self-test not supported 01b: ZQ may connect to V_{SS} or float 10b: ZQ may short to V_{DDQ} 11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V_{SS}, float, or short to V_{DDQ})	1-4
CA terminating rank	CATR	Read only	OP[7]	0b: ODT_CA pad for this rank is floating or tied to V_{ss} 1b: ODT_CA pad for this rank is tied to V_{DDQ}	5

Notes:
1. RZQI, if supported, will be set upon completion of the MRW ZQ INITIALIZATION CALIBRATION command.
2. If ZQ is connected to V_{DDQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ is not connected to V_{DDQ}, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assembly error. It is recommended that the assembly error be corrected.
3. In the case of possible assembly error, the device will default to factory trim settings for R_{ON}, and will ignore ZQ CALIBRATION commands. In either case, the device may not function as intended.
4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (i.e., 240Ω ±1%).
5. OP[7] is set at power-up, according to the state of the CA-ODT pad.

Table 11: MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL	

Table 12: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL Burst length	Write only	OP[1:0]	00b: BL = 16 sequential (default) 01b: BL= 32 sequential 10b: BL = 16 or 32 sequential (on-the-fly) 11b: Reserved	1, 6, 7
WR-PRE Write preamble length	Write only	OP[2]	0b: WR preamble = 1 * ^{t}CK (default) 1b: WR preamble = 2 * ^{t}CK	3, 6, 7
RD-PRE Read preamble type	Write only	OP[3]	0b: RD preamble = Static (default) 1b: RD preamble = Toggle	4, 6, 7
*n*WR Write-recovery for auto-precharge command	Write only	OP[6:4]	000b: *n*WR = 6 (default) 001b: *n*WR = 10 010b: *n*WR = 16 011b: *n*WR = 20 100b: *n*WR = 24 101b: *n*WR = 30 110b: *n*WR = 34 111b: *n*WR = 40	2, 6, 7
RD-PST Read post-amble length	Write only	OP[7]	0b: RD post-amble = 0.5 * ^{t}CK (default) 1b: RD post-amble = 1.5 * ^{t}CK	5, 6, 7

Notes:
1. Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in the command operands. See the Command Truth Table.
2. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal precharge after a write burst with auto precharge (AP) enabled. See Frequency Ranges for RL, WL, and *n*WR Settings table.
3. For WRITE operations at frequencies above CK = 400 MHz, OP[2] = 1b must be set to provide a 2 × ^{t}CK pre-amble. The memory controller will provide the 2 * ^{t}CK pre-amble (^{t}WPRE) for WRITE operations.
4. For READ operations, this bit must be set to select between a toggling preamble and a nontoggling preamble. (See the Preamble section.)
5. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional post-amble cycle is provided for the benefit of certain memory controllers.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
7. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the

FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Burst Mode Sequence

Table 13: Burst Sequence

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit READ Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
V	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
V	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
V	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
16-Bit WRITE Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32-Bit READ Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
0	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
0	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
1	**0**	**0**	**0**	**0**	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	**0**	**1**	**0**	**0**	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
1	**1**	**0**	**0**	**0**	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	**1**	**1**	**0**	**0**	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
32-Bit WRITE Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
1	**0**	**0**	**0**	**0**	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Notes:
1. First two left-most columns not shown include: Burst length bit = 16-bit or 32-bit; READ/WRITE operation bit = READ or WRITE operation.
2. C[1:0] are not present on the CA bus; they are implied to be zero.
3. The starting burst address on 64-bit (4*n*) boundaries.
4. C2–C3 must be set to 0 for all WRITE operations.

MR2:4

Table 14: MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Table 15: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RL READ latency	Write- only	OP[2:0]	RL and *n*RTP for DBI-RD Disabled (MR3 OP[6] = 0b) 000b: RL = 6, *n*RTP = 8 (default) 001b: RL = 10, *n*RTP = 8 010b: RL = 14, *n*RTP = 8 011b: RL = 20, *n*RTP = 8 100b: RL = 24, *n*RTP = 10 101b: RL = 28, *n*RTP = 12 110b: RL = 32, *n*RTP = 14 111b: RL = 36, *n*RTP = 16	1, 3, 4
			RL and *n*RTP for DBI-RD Enabled (MR3 OP[6] = 1b) 000b: RL = 6, *n*RTP = 8 001b: RL = 12,*n*RTP = 8 010b: RL = 16, *n*RTP = 8 011b: RL = 22, *n*RTP = 8 100b: RL = 28, *n*RTP = 10 101b: RL = 32, *n*RTP = 12 110b: RL = 36, *n*RTP = 14 111b: RL = 40, *n*RTP = 16	

Table 15: MR2 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition	Notes
WL WRITE latency	Write-only	OP[5:3]	WL Set A (MR2 OP[6] = 0b) 000b: WL = 4 (default) 001b: WL = 6 010b: WL = 8 011b: WL = 10 100b: WL = 12 101b: WL = 14 110b: WL = 16 111b: WL = 18	1, 3, 4
			WL Set B (MR2 OP[6] = 1b) 000b: WL = 4 001b: WL = 8 010b: WL = 12 011b: WL = 18 100b: WL = 22 101b: WL = 26 110b: WL = 30 111b: WL = 34	
WLS WRITE latency set	Write-only	OP[6]	0b: Use WL Set A (default) 1b: Use WL Set B	1, 3, 4
WR Lev Write leveling	Write-only	OP[7]	0b: Disable write leveling (default) 1b: Enable write leveling	2

Notes:
1. See Frequency Table for allowable frequency ranges for RL/WL/*n*WR.
2. After an MRW command to set the write-leveling enable bit (OP[7] = 1b), the device remains in the MRW state until another MRW command clears the bit (OP[7] = 0b). No other commands are allowed until the write-leveling enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
5. *n*RTP is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the *n*RTP value before starting a pre-charge.

Table 16: Frequency Ranges for RL, WL, *n*WR and *n*RTP Settings

READ Latency		WRITE Latency							
No DBI	w/DBI	Set A	Set B	*n*WR	*n*RTP	Lower Frequency Limit (>)	Upper Frequency Limit(≤)	Units	Notes
6	6	4	4	6	8	10	266	MHz	1–6
10	12	6	8	10	8	266	533		
14	16	8	12	16	8	533	800		
20	22	10	18	20	8	800	1066		
24	28	12	22	24	10	1066	1333		
28	32	14	26	30	12	1333	1600		
32	36	16	30	34	14	1600	1866		
36	40	18	34	40	16	1866	2133		

Notes:
1. The device should not be operated at a frequency above the upper frequency limit or below the lower frequency limit shown for each RL, WL or *n*WR value.
2. DBI for READ operations is enabled in MR3 OPO[6]. When MR3 OP[6] = 0, then the "No DBI" column should be used for READ latency. When MR3 OP[6] = 1, then the "w/DBI" column should be used for READ latency.
3. WRITE Latency Set A and Set B are determined by MR2 OP[6]. When MR2 OP[6] = 0, then Write Latency Set A should be used. When MR2 OP[6] = 1, then Write Latency Set B should be used.
4. The programmed value for *n*RTP is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a READ burst with AP (auto-pre-charge) enabled . It is determined by RU(^{t}RTP/^{t}CK).
5. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a WRITE burst with AP (auto precharge) enabled. It is determined by RU(^{t}WR/^{t}CK).
6. *n*RTP shown in this table is valid for BL16 only. For BL32, the device will add 8 clocks to the *n*RTP value before starting a precharge.

Table 17: MR3 I/O Configuration 1 (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			RFU	WR-PST	PU-CAL

Table 18: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PU-CAL (Pull-up calibration point)	Write-only	OP[0]	0b: V_{DDQ}/2.5	1
			1b: V_{DDQ}/3 (default)	
WR-PST (WR Post-Amble Length)		OP[1]	0b: WR Post-Amble=0.5*^{t}CK (default)	2
			1b: WR Post-Amble=1.5*^{t}CK	
PDDS (Pull-down drive strength)		OP[5:3]	000b: RFU	1, 3, 4
			001b: R_{ZQ}/1	
			010b: R_{ZQ}/2	
			011b: R_{ZQ}/3	
			100b: R_{ZQ}/4	
			101b: R_{ZQ}/5	
			110b:R_{ZQ}/6 (default)	
			111b: Reserved	
DBI-RD (DBI-read enable)		OP[6]	0b: Disabled (default)	3 , 4
			1b: Enabled	
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default)	3, 4
			1b: Enabled	

Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Recalibration may be required as voltage and temperature vary.
2. For frequencies 1066 MHz and above, WR PST length is 1.5^{t}CK
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 19: MR4 Device Temperature (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU	RFU	PPRE	RFU	Refresh Rate		

Table 20: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh Rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded 001b: 4x refresh 010b: 2x refresh 011b: 1x refresh 100b: 0.5x refresh 101b: 0.25x refresh, no derating 110b: 0.25x refresh, with derating 111b: SDRAM high temperature operating limit exceeded	1-4, 7-9
PPRE (Post-package repair entry/exit)	Write	OP[4]	0b: Exit PPR mode 1b: Enter PPR mode	5, 9
TUF (Temperature update flag)	Read-only	OP7	0b: OP[2:0] No change in OP[2:0] since last MR4 read (default) 1b: Change in OP[2:0] since last MR4 read	6-8

Notes:
1. The refresh rate for each MR4-OP[2:0] setting applies to ^{t}REFI, ^{t}REFIpb, and ^{t}REFW. OP[2:0] = 011b corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2] = 1, the device temperature is greater than 85°C.
2. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set OP[2:0] = 110b. See derating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]= 000b or 111b.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7] = 1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to 0.
7. OP[7] = 0 at power-up. OP[2:0] bits are undefined at power-up.
8. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
9. OP[4] and OP[5] are the only bits that can be written in this register. All other bits will be ignored by the device during an MRW command to this register.

MR5:8

Table 21: MR5 Basic Configuration 1 (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 22: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b: Micron All others: Refer to JESD-xxxx

Table 23: MR6 Basic Configuration 2 (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 24: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	0000 0000b: A version 0000 0001b: B version

Note: 1. MR6 is vendor-specific.

Table 25: MR7 Basic Configuration 3 (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 26: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	0000 0000b: A version 0000 0000b: B version

Note: 1. MR7 is vendor-specific.

Table 27: MR8 Basic Configuration 4 (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 28: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16*n* prefetch) All others: Reserved

Table 28: MR8 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition
Density	Read-only	OP[5:2]	0000b 4Gb per die (2Gb per channel) 0001b 6Gb per die (3Gb per channel) 0010b 8Gb per die (4Gb per channel) 0011b 12Gb per die (6Gb per channel) 0100b 16Gb per die (8Gb per channel) 0101b 24Gb per die (12Gb per channel) 0111b 32Gb per die (16Gb per channel) All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x16/channel All others: Reserved

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Table 29: MR9 Test Mode (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 30: MR10 Calibration (MA[7:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ RESET

Table 31: MR10 Op-Code Bit Definitions

Feature	Type	OP	Definition
ZQ Reset	Write-only	OP[0]	0b: Normal operation (default) 1b: ZQ reset

Notes:
1. See AC Timing table for calibration latency and timing.
2. If ZQ is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ reset) is supported. If ZQ is connected to V_{SS}, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

Table 32: Mode Register 11, ODT Control (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA_ODT			RFU	DQ ODT		

Table 33: MR11 Op-Code Bit Definitions

Notes 1-5 apply to entire table

Feature	Type	OP	Definition
DQ ODT DQ bus receiver On-Die-Termination	Write-only	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU
CA ODT CA bus receiver On-Die-Termination	Write-only	OP[6:4]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU All others: Reserved

Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 34: Mode Register 12 (MA[7:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR-CA	$V_{REF(CA)}$					

Table 35: MR12 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All others: Reserved	1-3, 5, 6

Table 35: MR12 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Data	Notes
VR_CA $V_{REF(CA)}$ range	Read/ Write	OP[6]	0b: $V_{REF(CA)}$ range[0] enabled 1b: $V_{REF(CA)}$ range[1] enabled (default)	1, 2, 4, 5, 6

Notes:
1. This register controls the $V_{REF(CA)}$ levels for frequency set point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting OP[6] appropriately.
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQs shall be set to 0. See the MRR Operation section.
3. A write to OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6] = 0b or sets FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(CA)}$ training section.
4. A write to OP[6] switches the device between two internal $V_{REF(CA)}$ ranges. The range (range[0] or range[1]) must be selected when setting the $V_{REF(CA)}$ register. The value, once set, will be retained until overwritten or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 36: Mode Register 13 Register (MA[7:0] = 0Dh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RFU	VRCG	VR0	RFU	CBT

Table 37: MR13 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
CBT Command bus training	Write-only	OP[0]	0b: Normal operation (default) 1b: Command bus training mode enabled	1
RFU		OP[1]	RFU	
VRO V_{REF} output		OP[2]	0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ and V_{REFDQ} values on DQ bits	2
VRCG V_{REF} current generator		OP[3]	0b: Normal operation (default) 1b: Fast response (high current) mode	3
DMD Data mask Disable		OP[5]	0b: DATA MASK operation enabled (default) 1b: DATA MASK operation disabled	4
FSP-WR Frequency Set Point Write enable		OP[6]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	5
FSP-OP Frequency Set Point Operation mode		OP[7]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	6

Notes:
1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the device will output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltage on DQ pins. Only the "active" frequency set point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for VREF output are vendor specific.
3. When OP[3] = 1, the V_{REF} circuit uses a high current mode to improve V_{REF} settling time.
4. When enabled (OP[5] = 0b) data masking is enabled for the device. When disabled (OP[5] = 1b), the device will ignore any mask patterns issued during a MASKED WRITE command. See the Data Mask section for more information.
5. FSP-WR determines which frequency set point registers are accessed with MRW and MRR commands for the following functions: $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range, CA ODT enable, CA ODT value, DQ ODT enable, DQ ODT value, DQ calibration point, WL, RL, *n*WR, read and write preamble, read postamble and DBI enables.
6. FSP-OP determines which frequency set point register values are currently used to specify device operation for the following functions: $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range, CA ODT enable, CA ODT value, DQ ODT enable, DQ ODT value, DQ calibration point, WL, RL, *n*WR, read and write preamble, read postamble, and DBI enables.

Table 38: Mode Register 14 (MA[7:0] = 0Eh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	V_{RDQ}	V_{REFDQ}					

Table 39: MR14 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
V_{REFDQ} V_{REFDQ} setting	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All Others: Reserved	1-3, 5-6
V_{RDQ} V_{REFDQ} range		OP[6]	0b: V_{REFDQ} range[0] enabled 1b: V_{REFDQ} range[1] enabled (default)	1-2, 4-6

Notes:
1. This register controls the V_{REFDQ} levels for frequency set point[1:0]. Values from either V_{RDQ}[vendor defined] or V_{RDQ}[vendor defined] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQs shall be set to 0. See the MRR Operation section.
3. A write to OP[5:0] sets the internal V_{REFDQ} level for FSP[0] when MR13 OP[6] = 0b, or sets FSP[1] when MR13 OP[6] = 1b. The time required for V_{REFDQ} to reach the set level depends on the step size from the current level to the new level. See the V_{REFDQ} training section.
4. A write to OP[6] switches the device between two internal V_{REFDQ} ranges. The range (range[0] or range[1]) must be selected when setting the V_{REFDQ} register. The value, once set, will be retained until overwritten, or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 40: V_{REF} Setting for Range[0] and Range[1]

Notes 1-3 apply to entire table

Function	OP	Range[0] Values		Range[1] Values	
		$V_{REF}CA$ (% of V_{DD2})		$V_{REF}CA$ (% of V_{DD2})	
		$V_{REF}DQ$ (% of V_{DDQ})		$V_{REF}DQ$ (% of V_{DDQ})	
V_{REF} Setting for MR12 and MR14	OP[5:0]	000000b: 10.0%	011010b: 20.4%	000000b: 22.0%	011010b: 32.4%
		000001b: 10.4%	011011b: 20.8%	000001b: 22.4%	011011b: 32.8%
		000010b: 10.8%	011100b: 21.2%	000010b: 22.8%	011100b: 33.2%
		000011b: 11.2%	011101b: 21.6%	000011b: 23.2%	011101b: 33.6%
		000100b: 11.6%	011110b: 22.0%	000100b: 23.6%	011110b: 34.0%
		000101b: 12.0%	011111b: 22.4%	000101b: 24.0%	011111b: 34.4%
		000110b: 12.4%	100000b: 22.8%	000110b: 24.4%	100000b: 34.8%
		000111b: 12.8%	100001b: 23.2%	000111b: 24.8%	100001b: 35.2%
		001000b: 13.2%	100010b: 23.6%	001000b: 25.2%	100010b: 35.6%
		001001b: 13.6%	100011b: 24.0%	001001b: 25.6%	100011b: 36.0%
		001010b: 14.0%	100100b: 24.4%	001010b: 26.0%	100100b: 36.4%
		001011b: 14.4%	100101b: 24.8%	001011b: 26.4%	100101b: 36.8%
		001100b: 14.8%	100110b: 25.2%	001100b: 26.8%	100110b: 37.2%
		001101b: 15.2%	100111b: 25.6%	001101b: 27.2% default	100111b: 37.6%
		001110b: 15.6%	101000b: 26.0%	001110b: 27.6%	101000b: 38.0%
		001111b: 16.0%	101001b: 26.4%	001111b: 28.0%	101001b: 38.4%
		010000b: 16.4%	101010b: 26.8%	010000b: 28.4%	101010b: 38.8%
		010001b: 16.8%	101011b: 27.2%	010001b: 28.8%	101011b: 39.2%
		010010b: 17.2%	101100b: 27.6%	010010b: 29.2%	101100b: 39.6%
		010011b: 17.6%	101101b: 28.0%	010011b: 29.6%	101101b: 40.0%
		010100b: 18.0%	101110b: 28.4%	010100b: 30.0%	101110b: 40.4%
		010101b: 18.4%	101111b: 28.8%	010101b: 30.4%	101111b: 40.8%
		010110b: 18.8%	110000b: 29.2%	010110b: 30.8%	110000b: 41.2%
		010111b: 19.2%	110001b: 29.6%	010111b: 31.2%	110001b: 41.6%
		011000b: 19.6%	110010b: 30.0%	011000b: 31.6%	110010b: 42.0%
		011001b: 20.0%	All Others: Reserved	011001b: 32.0%	All Others: Reserved

Notes:
1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the $V_{REF(CA)}$ or V_{REFDQ} levels in the device.
2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency set points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation or between different high-frequency settings which may use different terminations values.

Table 41: MR15 Register Information (MA[7:0] = 0Fh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Table 42: MR15 Op-code Bit Definition

Feature	Type	OP	Definition	Notes
Lower-byte invert for DQ calibration	Write-Only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h	1–3

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQs. Example: If MR15 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DM[0] is not inverted and always transmits the "true" data contained in MR32 and MR40.
3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3-OP[6].

Table 43: MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMIO	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No-Invert	OP4	OP5	OP6	OP7

Table 44: MR16 PASR Bank Mask (MA[7:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Bank Mask							

Table 45: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: Band refresh enabled (default) 1b: Bank refresh disabled

$OP[_n]$	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3

OP[$_n$]	Bank Mask	8-Bank SDRAM
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:
1. When a mask bit is asserted (OP[*n*] = 1), refresh to that bank is disabled.
2. PASR bank masking is on a per-channel basis; the two channels on the die may have different bank masking.

Table 46: MR17 PASR Segment Mask (MA[7:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 47: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: Segment refresh enabled (default) 1b: Segment refresh disabled

Table 48: MR17 PASR Segment Mask

Segment	OP	Segment Mask	4Gb R[13:11]	6Gb R[14:12]	8Gb R[14:12]	12Gb R[15:13]	16Gb R[15:13]	24Gb TBD	32Gb TBD
0	0	XXXXXXX1	000b						
1	1	XXXXXX1X	001b						
2	2	XXXXX1XX	010b						
3	3	XXXX1XXX	011b						
4	4	XXX1XXXX	100b						
5	5	XX1XXXXX	101b						
6	6	X1XXXXXX	110b	Not allowed	110b	Not allowed	110b	Not allowed	110b
7	7	1XXXXXXX	111b		111b		111b		111b

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is “Don’t Care” for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
3. For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (= 00b).

Table 49: MR18 Register Information (MA[7:0]=12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count - LSB							

Table 50: MR18 LSB DQS Oscillator Count

Notes 1–3 apply to entire table

Function	Type	OP	Definition
DQS oscillator (WR training DQS oscillator)	Read-only	OP[7:0]	0h:- FFh LSB DRAM DQS oscillator count

Notes:
1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. The value in this register is reset each time an MPC command is issued to start in the DQS oscillator counter.

Table 51: MR19 Register Information (MA[7:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count – MSB							

Table 52: MR19 DQS Oscillator Count

Notes 1–3 apply to the entire table

Function	Type	OP	Definition
DQS oscillator count – MSB (WR training DQS oscillator)	Read-only	OP[7:0]	0h:- FFh MSB DRAM DQS oscillator count

Notes:
1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. A new MPC-1 [start DQS oscillator] should be issued to reset the contents of MR18/MR19.

Table 53: MR20 Register Information (MA[7:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-byte invert register for DQ calibration							

Table 54: MR20 Register Information

Notes 1–2 apply to entire table

Function	Type	OP	Definition
Upper-byte invert for DQ calibration	Write	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane 0b: Do not invert 1b: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h

Notes:
1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQs. For example, if MR20 OP[7:0] = 00010101b, the DQ calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DM[1] is not inverted and always transmits the true data contained in MR32 and MR40.
3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 55: MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 56: MR21 Register Information (MA[7:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Table 57: MR22 Register Information (MA[7:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTD-CA	ODTE-CS	ODTE-CK	CODT		

Table 58: MR22 Register Information

Function	Type	OP	Data	Notes
SOC ODT (controller ODT value for VOH calibration)	Write-only	OP[2:0]	000b: Disable (default) 001b: $R_{ZQ}/1$ 010b: $R_{ZQ}/2$ 011b: $R_{ZQ}/3$ 100b: $R_{ZQ}/4$ 101b: $R_{ZQ}/5$ 110b: $R_{ZQ}/6$ 111b: RFU	1, 2, 3

Table 58: MR22 Register Information (Continued)

Function	Type	OP	Data	Notes
ODTF-CK (CK ODT force for non-terminating rank)	Write-only	OP[3]	0b: ODT-CK override disabled (default) 1b: ODT-CK override enabled	2, 3, 4, 6
ODTF-CS (CS ODT force for non-terminating rank)	Write-only	OP[4]	0b: ODT-CS override disabled (default) 1b: ODT-CS override enabled	2, 3, 5, 6
ODTD-CA (CA ODT termination disable)	Write-only	OP[5]	0b: ODT-CA obeys ODT_CA bond pad (default) 1b: ODT-CA disabled	2, 3, 6, 7

Notes:
1. All values are typical.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
4. When OP[3] = 1 the CK signals will be terminated to the value set by MR11 OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more devices but CK is not, enabling CK to terminate on all devices.
5. When OP[4] = 1 the CS signal will be terminated to the value set by MR11 OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more devices but CS is not, enabling CS to terminate on all devices.
6. For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared command bus signals.
7. When OP[5] = 0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11 OP[6:4] is valid and disable termination when ODT_CA is LOW or MR11 OP[6:4] is disabled. When OP[5] = 1, termination for CA[5:0] is disabled regardless of the state of the ODT_CA bond pad or MR11 OP[6:4].

Table 59: MR23 Register Information (MA[7:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run time setting							

Table 60: MR23 Register Information

Notes 1–2 apply to entire table

Function	Type	OP	Data
DQS interval timer run time	Write-only	OP[7:0]	00000000b: Disabled (default) 00000001b: DQS timer stops automatically at the 16th clock after timer start 00000010b: DQS timer stops automatically at the 32nd clock after timer start 00000011b: DQS timer stops automatically at the 48th clock after timer start 00000100b: DQS timer stops automatically at the 64th clock after timer start --------- Through --------- 00111111b: DQS timer stops automatically at the (63 * 16)th clock after timer start 01XXXXXXb: DQS timer stops automatically at the 2048th clock after timer start 10XXXXXXb: DQS timer stops automatically at the 4096th clock after timer start 11XXXXXXb: DQS timer stops automatically at the 8192nd clock after timer start

Notes:
1. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) stops the DQS interval timer in the case of MR23 OP[7:0] = 00000000b.
2. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) is illegal with valid non-zero values in MR23 OP[7:0].

Table 61: MR24 Register Information (MA[7:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR Mode	TRR BAn			Unlimited MAC	MAC value		

Table 62: MR24 Register Information

Function	Type	OP	Data	Notes
MAC value	Read	OP[2:0]	000b: Unknown (OP[3] = 0) or Unlimited (OP[3]=1) 001b: 700K 010b: 600K 011b: 500K 100b: 400K 101b: 300K 110b: 200K 111b: Reserved	1

Table 62: MR24 Register Information (Continued)

Function	Type	OP	Data	Notes
Unlimited MAC	Read	OP[3]	0b: OP[2:0] defines the MAC value 1b: Unlimited MAX value	 1, 2
TRR Mode BAn	Write	OP[6:4]	000b: Bank 0 001b: Bank 1 010b: Bank 2 011b: Bank 3 100b: Bank 4 101b: Bank 5 110b: Bank 6 111b: Bank 7	
TRR Mode	Write	OP[7]	0b: Disabled (default) 1b: Enabled	

Notes:
1. Unknown means that the device is not tested for ^{t}MAC and pass/fail values are unknown. Unlimited means that there is no restriction on the number of activates between refresh windows
2. MR24 OP[2:0] set to 000b.

Table 63: MR25 Register Information (MA[7:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Table 64: MR25 Register Information

Function	Type	OP	Data
PPR resources	Read-only	OP[7:0]	0b: PPR resource is not available 1b: PPR resource is available

Note:
1. When OP[n] = 0, there is no PPR resource available for that bank. When OP[n] = 1, there is a PPR resource available for that bank, and PPR can be initiated by the controller.

Table 65: MR26:31 Register Information (MA[7:0] = 1Ah–1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table 66: MR32 Register Information (MA[7:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern A (default = 5Ah)							

Table 67: MR32 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Read/ write	OP[7:0]	Xb: An MPC command issued with OP[6:0] = 0000011b causes the device to return the DQ calibration pattern contained in this register and (followed by) the contents of MR40. A default pattern 5AH is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the MR32/MR40 data pattern for a given DQ (see MR15/MR20 for more information).	1, 2, 3

Notes:
1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when DQ read calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, the first bit transmitted is a 1 followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 68: DQ Read Calibration Bit Ordering and Inversion Example – MR32 = 1Ch, MR40 = 59h, MR15 = MR20 = 55h

	Bit Sequence																
Pin	Invert	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ0	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ1	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ2	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ3	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI0	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ4	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ5	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ6	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ7	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ8	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ9	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ10	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ11	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI1	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

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Table 68: DQ Read Calibration Bit Ordering and Inversion Example – MR32 = 1Ch, MR40 = 59h, MR15 = MR20 = 55h (Continued)

Pin	Bit Sequence																
	Invert	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ12	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ13	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ14	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ15	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

Table 69: MR33:39 Register Information (MA[7:0] = 21h–27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 70: MR40 Register Information (MA[7:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern B (default = 3Ch)							

Table 71: MR40 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: A default pattern 3Ch is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1, 2, 3

Notes:
1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ read calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, the first bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR22 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 72: MR41:47 Register Information (MA[7:0] = 29h–2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 73: MR48:63 Register Information (MA[7:0] = 30h–3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Commands and Timing

Commands transmitted on the CA bus are encoded into two parts and are latched on two consecutive rising edges of the clock. This is called 2-tick CA capture because each command requires two clock edges to latch and decode the entire command.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be either reset by asserting the RESET_n command or powered down and then restarted using the specified initialization sequence before normal operation can continue.

Table 74: Command Truth Table

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data.

Note:

MASKED WRITE-1 command only supports BL16. For MASKED WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).

Command	SDR Command Pins		SDR CA Pins							CK Edge	Notes
	CKE										
	CK_t (*n*-1)	CK_t(*n*)	CS	CA0	CA1	CA2	CA3	CA4	CA5		
MRW-1	H	H	H	L	H	H	L	L	OP7	R1	1, 2, 11
			L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
MRW-2	H	H	H	L	H	H	L	H	OP6	R1	1, 2, 11
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
MRR-1	H	H	H	L	H	H	H	L	V	R1	1, 2, 12
			L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
REFRESH (all/per bank)	H	H	H	L	L	L	H	L	AB	R1	1, 2, 4, 5
			L	BA0	BA1	BA2	V	V	V	R2	
ENTER SELF REFRESH	H	H	H	L	L	L	H	H	V	R1	1,2
			L	V						R2	
ACTIVATE-1	H	H	H	H	L	R12	R13	R14	R15	R1	1, 2, 4, 11
			L	BA0	BA1	BA2	V	R10	R11	R2	
ACTIVATE-2	H	H	H	H	H	R6	R7	R8	R9	R1	1, 11
			L	R0	R1	R2	R3	R4	R5	R2	
WRITE-1	H	H	H	L	L	H	L	L	BL	R1	1, 2, 4, 6, 7, 9
			L	BA0	BA1	BA2	V	C9	AP	R2	

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Table 74: Command Truth Table (Continued)

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data.

Note:

MASKED WRITE-1 command only supports BL16. For MASKED WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).

Command	SDR Command Pins		SDR CA Pins							CK Edge	Notes
	CKE										
	CK_t (*n*-1)	CK_t(*n*)	CS	CA0	CA1	CA2	CA3	CA4	CA5		
EXIT SELF REFRESH	H	H	H	L	L	H	L	H	V	R1	1, 23
			L	V						R2	
MASKED WRITE-1	H	H	H	L	L	H	H	L	L	R1	1, 2, 4, 6 on page 0 (page 0), 67, 9
			L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	H	H	L	L	H	H	H	V	R1	1, 2
			L	V						R2	
READ-1	H	H	H	L	H	L	L	L	BL	R1	1, 2, 4, 6, 7, 9
			L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (WRITE-2, MASKED WRITE-2, READ-2, MRR-2, MPC (except NOP)	H	H	H	L	H	L	L	H	C8	R1	1, 8, 9
			L	C2	C3	C4	C5	C6	C7	R2	
PRECHARGE (all/per bank)	H	H	H	L	L	L	L	H	AB	R1	1, 2, 4, 5
			L	BA0	BA1	BA2	V	V	V	R2	
MPC-1 (TRAIN, NOP)	H	H	H	L	L	L	L	L	OP6	R1	1, 2, 13
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
MAINTAIN PD (NOP)	L	L	X	X						R1	1, 2
DESELECT	H	H	L	X						R1	1, 2
ENTER POWER DOWN	H	L	L	V						R1	1, 2
	L		L	V						R2	
EXIT PD	L	H	L	V						R1	1, 2, 3
	H		L	V						R2	

Notes: 1. All commands except for DESELECT and MAINTAIN PD/SELF REFRESH are two clock cycles and are defined by the current state of CS, CA[5:0], and CKE at the rising edge of the

clock. DESELECT and MAINTAIN PD/SELF REFRESH commands are one clock cycle and are not latched by the device.

2. V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.
3. POWER-DOWN ENTRY/EXIT and SELF REFRESH and POWER-DOWN within SELF REFRESH are asynchronous commands based on the states of CKE and CS.
4. Bank addresses BA[2:0] determine which bank is to be operated upon.
5. AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all banks, and the bank addresses are "Don't Care."
6. AP HIGH during a WRITE-1, MASKED-WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.
7. When enabled in the mode register, BL HIGH during a WRITE-1, MASKED-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If burst-length-on-the-fly is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.
8. For CAS-2 commands (WRITE-2, MASKED-WRITE-2, READ-2, MRR-2, or MPC [except NOP]), C[1:0] are not transmitted on the CA bus and are assumed to be LOW by the device. For WRITE commands (WRITE-2, MASKED-WRITE-2), C[3:2] must be driven LOW. For CAS-2 commands after MRR-1 or MPC-1, all of the address bits are ignored but must be driven to a valid level.
9. WRITE-1, MASKED-WRITE-1, READ-1, MRR-1, or MPC (except for NOP) commands must be followed by a CAS-2 command consecutively without any other command between them (that is, the next command after READ-1 must be CAS-2). WRITE-1, MASKED-WRITE-1, READ-1, MRR-1, or MPC (except for NOP) commands must be issued before issuing a CAS-2 command.
10. The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
11. The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.
12. The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.
13. The MPC-1 command for READ or WRITE training operations must be followed by the CAS-2 command consecutively without any other commands between them. The MPC-1 command must be issued prior to the CAS-2 command.

Table 75: CKE Truth Table

Notes 1–3 apply to entire table; L = LOW; H = HIGH; X = “Don’t Care”

Current State	CKE*n*-1	CKE*n*	Command *n*	Operation *n*	Next State	Notes
Active power-down	L	L	X	Maintain active power-down	Active power-down	
	L	H	DESELECT	Exit active power-down	Active	4, 5

Table 75: CKE Truth Table (Continued)

Notes 1–3 apply to entire table; L = LOW; H = HIGH; X = "Don't Care"

Current State	CKE*n*-1	CKE*n*	Command *n*	Operation *n*	Next State	Notes
Idle power-down	L	L	X	Maintain idle power-down	Idle power-down	
	L	H	DESELECT	Exit idle power-down	Idle	4, 5
Self refresh	L	L	X	Maintain power-down state within self refresh	Self refresh	
	L	H	DESELECT	Exit SREF power-down, enable command decode	Self refresh	4, 5, 6
	H	L	DESELECT	Enter SREF power-down, disable command decode	Self refresh	4, 6
	H	H	See note 6	See note 6	Self refresh	6
Bank(s) active	H	L	DESELECT	Enter active power-down	Active power-down	4
All banks idle	H	L	DESELECT	Enter idle power-down	Idle power-down	4
Resetting	H	L	NOP (deselect)	Enter resetting power-down	Resetting power-down	
Command entry	H	H	Refer to the command table			

Notes:
1. CKE is an asynchronous input only and has no relationship to CK.
2. Current state = the state of the device immediately prior to toggle of CKE.
3. CKE_{n-1} = the logic state of CKE prior to a CKE toggle event; CKE_n = the state of CKE after the toggle event.
4. DESELECT is the only valid command that can be present on the bus when CKE is toggled.
5. Power-down exit time (^{t}XP) must elapse before a command other than DESELECT is issued. The clock must toggle at least twice during the ^{t}XP period and must be stable before issuing a command.
6. When the device is in self-refresh, only MRR, MRW, or MPC commands are allowed. Certain restrictions apply to changing register contents via an MRW command during SREF. See MODE REGISTER WRITE for more information.

Command Input Signal Timing

The base setup and hold values for input signals is measured from CK to the V_{IL}/V_{IH} level of the signal.

Derating to the V_{REF} level can be found in the Setup/Hold Derating tables in AC Timing.

Figure 6: Command Input Timing

TBD

Timing Restrictions for Command Sequences

When sequencing commands to the device, the timing between commands must be observed as shown in the tables below. Timing is different for commands that target the same bank than for commands that target different banks, as shown below.

Table 76: Command Sequence Timing Restriction – Same Bank

Current Command	Next Command					Units	Notes
	ACTIVE	READ	WRITE	MASK WRITE[1]	PRECHARGE		
ACTIVE	Illegal	RU (^{t}RCD/^{t}CK)	RU(^{t}RCD/^{t}CK)	RU(^{t}RCD/^{t}CK)	RU(^{t}RAS/^{t}CK)	^{t}CK	
READ	Illegal	^{t}CCD	RL + RU [^{t}DQSCK (MAX)/^{t}CK] + BL/2 - WL + ^{t}WPRE + ^{t}RPST	RL + RU [^{t}DQSCK (MAX)/^{t}CK] + BL/2 - WL + ^{t}WPRE + ^{t}RPST	BL/2 + MAX[8, RU(^{t}RTP/^{t}CK] - 8	^{t}CK	2, 3, 4
WRITE	Illegal	WL + 1 + BL/2 + RU^{t}WTR/ ^{t}CK)	^{t}CCD	^{t}CCDMW	WL + 1 + BL/2 + RU(^{t}WR/^{t}CK)	^{t}CK	2, 3
MASK WRITE	Illegal	WL + 1 + BL/2 + RU^{t}WTR/ ^{t}CK)	^{t}CCD	^{t}CCDMW	WL + 1 + BL/2 + RU(^{t}WR/^{t}CK)	^{t}CK	2
PRECHARGE	RU(^{t}RPpb/^{t}CK) or RU(^{t}RPab/^{t}CK	Illegal	Illegal	Illegal	4	^{t}CK	

Notes:
1. MASK WRITE commands only support BL16 operations.
2. ^{t}CCD = BL/2.
3. ^{t}CCDMW = 4 * ^{t}CCD.
4. Add 8*n* CK if BL32 (static or on-the-fly) is selected for a WRITE command followed by a MASK WRITE command.

Table 77: Command Sequence Timing Restriction – Different Bank

Current Command	Next Command					Units	Notes
	ACTIVE	READ	WRITE	MASK WRITE[1]	PRECHARGE		
ACTIVE	RU (^{t}RRD/^{t}CK)	4	4	4	2	^{t}CK	
READ	4	^{t}CCD	RL + RU [^{t}DQSCK (MAX)/^{t}CK] + BL/2 - WL + ^{t}WPRE + ^{t}RPST	RL + RU [^{t}DQSCK (MAX)/^{t}CK] + BL/2 - WL + ^{t}WPRE + ^{t}RPST	2	^{t} CK	2
WRITE	4	WL + 1 + BL/2 + RU(^{t}WTR/ ^{t}CK)	^{t}CCD	^{t}CCD	2	^{t}CK	2, 3
MASK WRITE	4	WL + 1 + BL/2 + RU(^{t}WTR/ ^{t}CK)	^{t}CCD	^{t}CCD	2	^{t}CK	2
PRECHARGE	4	4	4	4	4	^{t} CK	

Notes:
1. MASK WRITE commands only support BL16 operations.
2. ^{t}CCD = BL/2.
3. Add 8*n* CK if BL32 (static or on-the-fly) is selected for a WRITE command followed by a MASK WRITE command.

ACTIVATE Command

The ACTIVATE command must be executed before a READ or WRITE command can be issued. The ACTIVATE command is issued in two parts: The bank and upper-row addresses are entered with activate-1 and the bank and lower-row addresses are entered with activate-2. Activate-1 and activate-2 are executed by strobing CS HIGH while setting CA[5:0] at valid levels (see Command table) at the rising edge of CK.

The bank addresses (BA[2:0]) are used to select the desired bank. The row addresses (R0-R15) are used to determine which row to activate in the selected bank. The ACTIVATE-2 command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at time ^{t}RCD after the ACTIVATE-2 command is sent. Once a bank has been activated, it must be precharged to close the active row before another ACTIVATE-2 command can be applied to the same bank. The bank active and precharge times are defined as^{t}RAS and ^{t}RP, respectively. The minimum time interval between successive ACTIVATE-2 commands to the same bank is determined by the row cycle time of the device (^{t}RC). The minimum time interval between ACTIVATE-2 commands to different banks is ^{t}RRD.

Certain restrictions must be observed for bank ACTIVATE and REFpb operations.

- Four-activate window (^{t}FAW): No more than 4 banks may be activated (or refreshed, in the case of REFpb) per channel in a rolling ^{t}FAW window. Convert to clocks by dividing ^{t}FAW[ns] by ^{t}CK[ns] and rounding up to the next integer value. As an example of the rolling window, if RU[(^{t}FAW/^{t}CK)] is 64 clocks, and an ACTIVATE command is issued on clock N, no more than three additional ACTIVATE commands may be issued between clock N + 1 and N + 63. REFpb also counts as bank activation for the purposes of ^{t}FAW.
- 8-bank per channel, precharge all banks (AB) allowance: ^{t}RP for a PRECHARGE ALL BANKS command for an 8-bank device must equal ^{t}RPab, which is greater than ^{t}RPpb.

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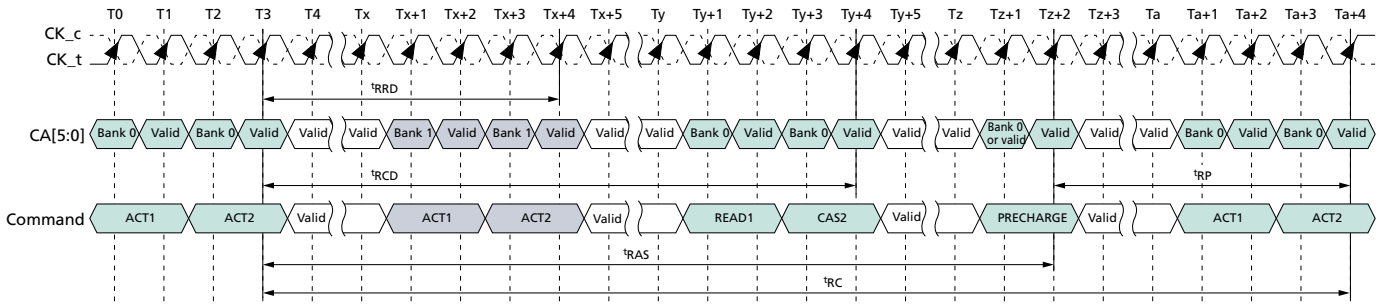
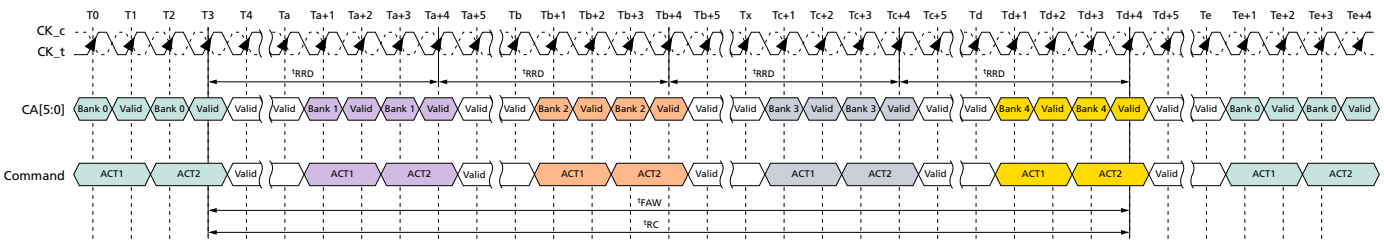
Figure 7: ACTIVATE Command



Note: 1. ^{t}RP may be all bank or per bank.

Figure 8: tFAW Timing



Note: REFpb command can be substituted for one of the ACTIVATE commands for the purposes of tFAW.

Note: 1. REFpb may be substituted for one of the ACTIVATE commands for the purposes of tFAW.

Read and Write Access Modes

After a bank has been activated, a READ or WRITE command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) on the rising edge of CK.

The device provides a fast column access operation. A single READ or WRITE command will initiate a burst READ or WRITE operation, where data is transferred to/from the device on successive clock cycles. Burst interrupts are not allowed; however, the optimal burst length may be set on the fly (see Command Truth Table).

Burst READ Operation

A burst READ command is initiated with CKE, CS, and CA[5:0] asserted to the proper state on the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be 0; therefore, the starting burst address is always a multiple of four (ie.g., 0x0, 0x4, 0x8, 0xC).

The READ latency (RL) is defined from the last rising edge of the clock that completes a READ command (e.g., the second rising edge of the CAS-2 command) to the rising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid data is available RL * ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of clock that completes a READ command.

The data strobe output is driven ^{t}RPRE before the first valid rising strobe edge. The first data bit of the burst is synchronized with the first valid (post-preamble) rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst, the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle post-amble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c.

Figure 9: Read Output Timing

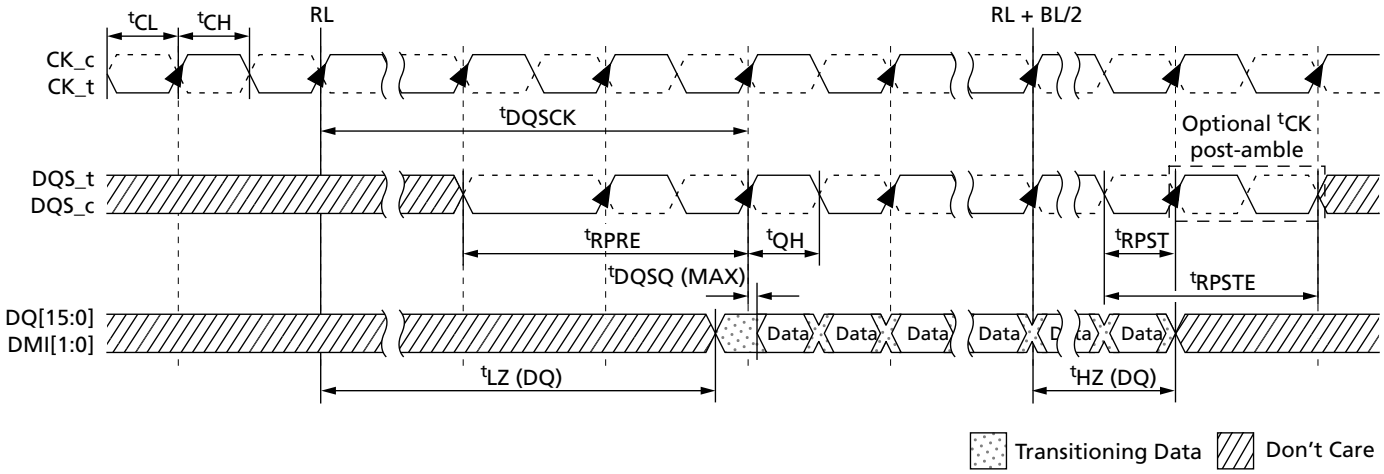


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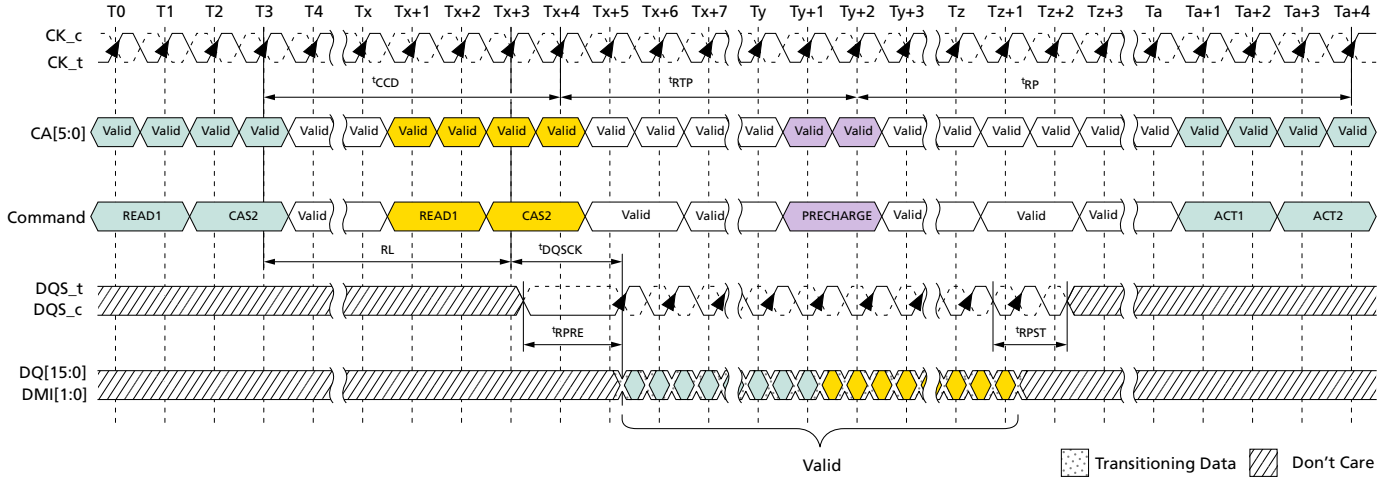
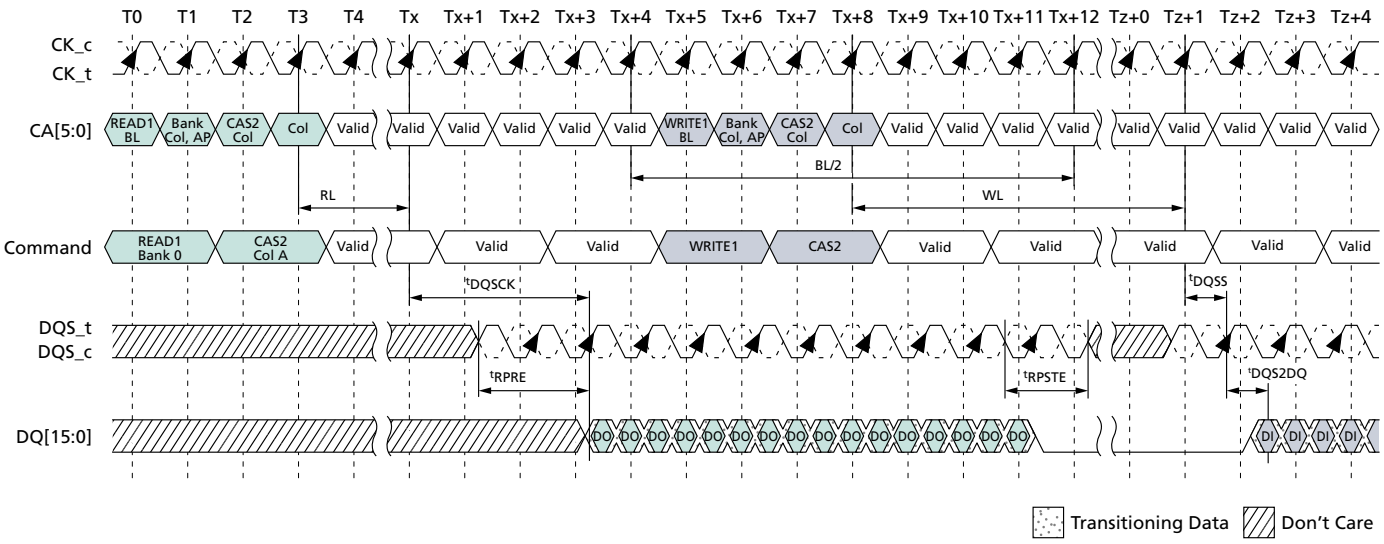
Figure 10: Burst Read Timing



Note: 1. tDQSCK may span multiple clock periods.

Figure 11: Burst Read Followed by Burst Write



Note: 1. The minimum time from a burst READ command to a burst WRITE command is defined by the READ latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK (MAX)/tCK) + BL/2 - WL + tWPRE + tRPST.

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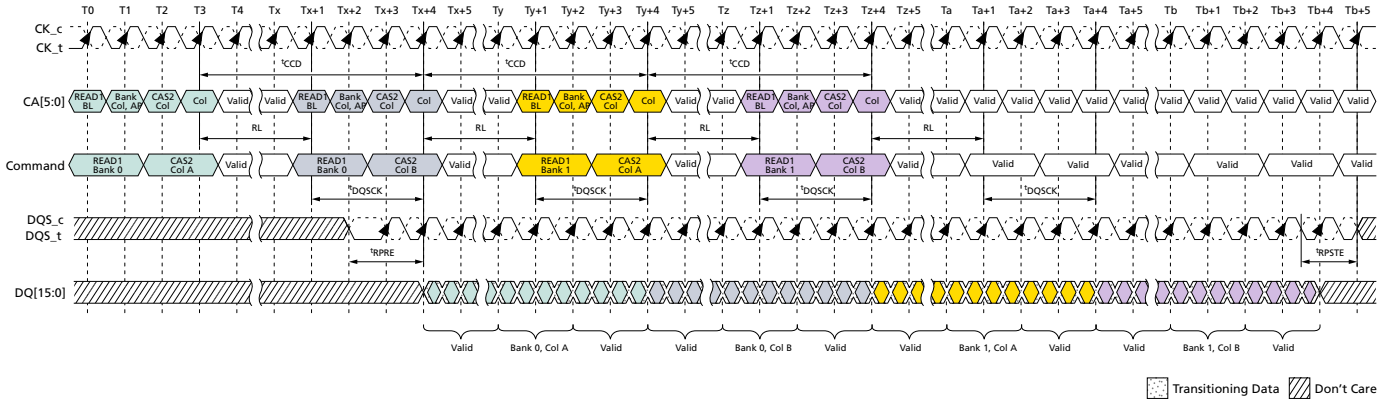
Figure 12: Seamless Burst Read



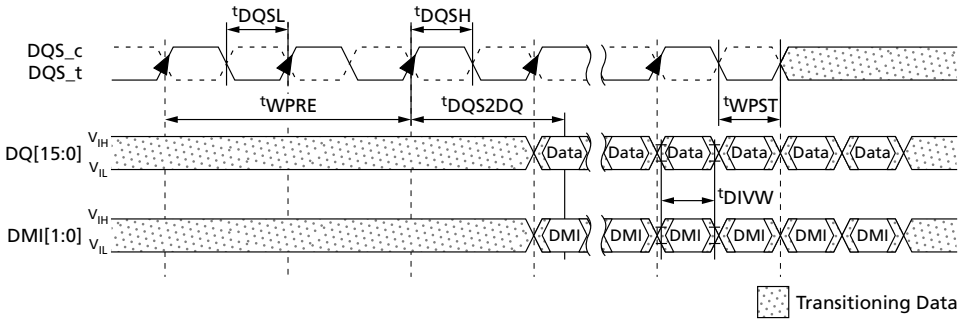
Note: 1. The seamless burst READ operation is supported by placing a READ command at every ^{t}CCD interval for BL16 (or every 2 x ^{t}CCD for BL32). A seamless burst read can access any open bank.

Burst WRITE Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus and are assumed to be zero so that the starting column burst address is always aligned with a 32-byte boundary. The WRITE latency (WL) is defined from the last rising edge of the clock that completes a WRITE command (for example, the second rising edge of the CAS-2 command) to the rising edge of the clock from which ^{t}DQSS is measured. The first valid latching edge of DQS must be driven WL * ^{t} CK + ^{t}DQSS after the rising edge of clock that completes a WRITE command.

The device uses an unmatched DQS DQ path for lower power, so the DQS strobe must arrive at the SDRAM ball prior to the DQ signal by ^{t}DQS2DQ . The DQS strobe output must be driven ^{t}WPRE before the first valid rising strobe edge. The ^{t}WPRE preamble is required to be 1 x ^{t}CK at lower speeds and 2 x ^{t}CK at higher speeds (frequency TBD). The DQS strobe must be trained to arrive at the DQ pad latch center-aligned with the DQ data. The DQ data must be held for ^{t}DIVW, and the DQS must be periodically trained to stay roughly centered in the ^{t}DIVW. Burst data is captured by the SDRAM on successive edges of DQS until the 16- or 32-bit data burst is complete. The DQS strobe must remain active (toggling) for ^{t}WPST (write postamble) after the completion of the burst write. After a burst WRITE operation, ^{t}WR must be satisfied before a PRECHARGE command to the same bank can be issued. Signal input timings are measured relative to the cross point of DQS_t and DQS_c.

Figure 13: Data Input Write Timing



Proposal

Figure 14: Burst WRITE Operation

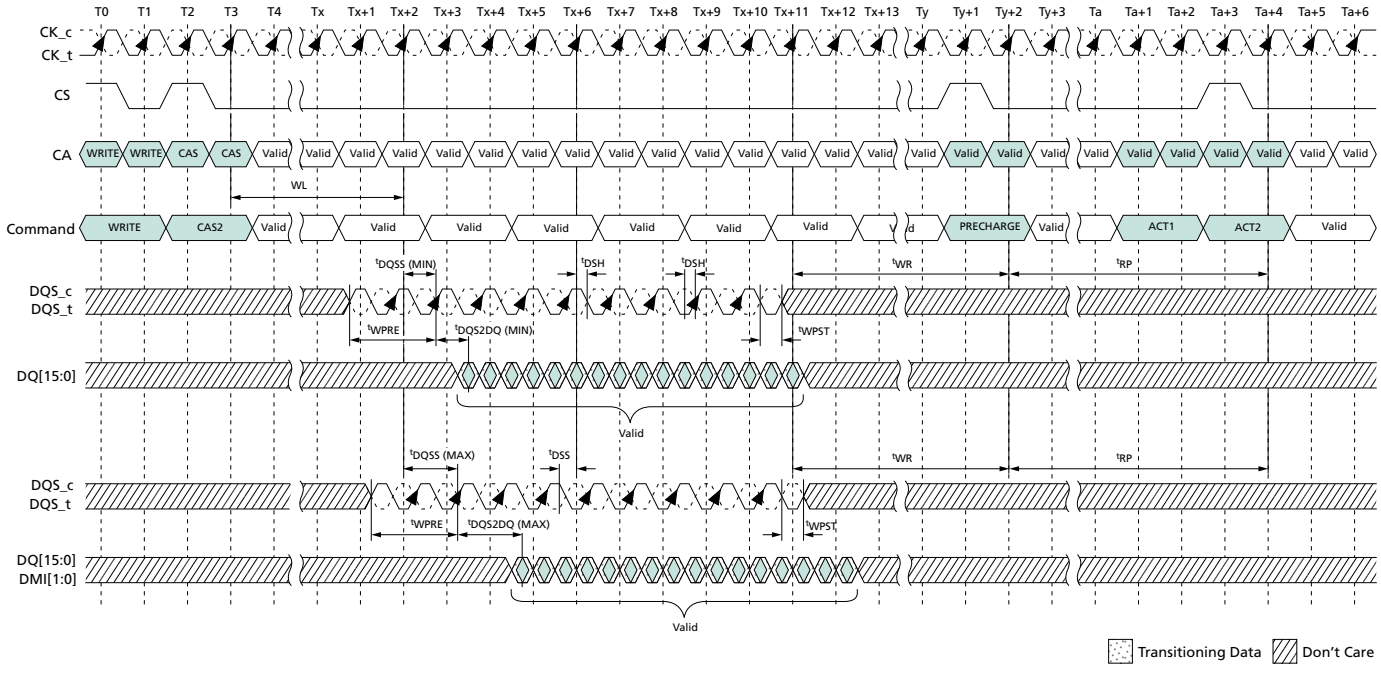
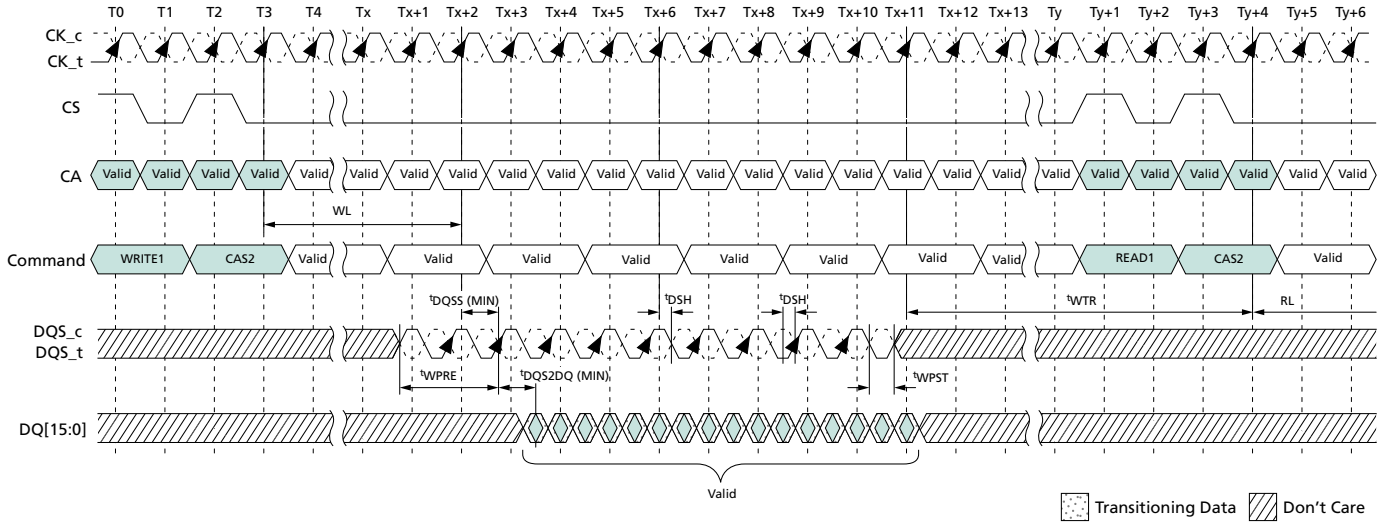


Figure 15: Burst Write Followed by Burst Read



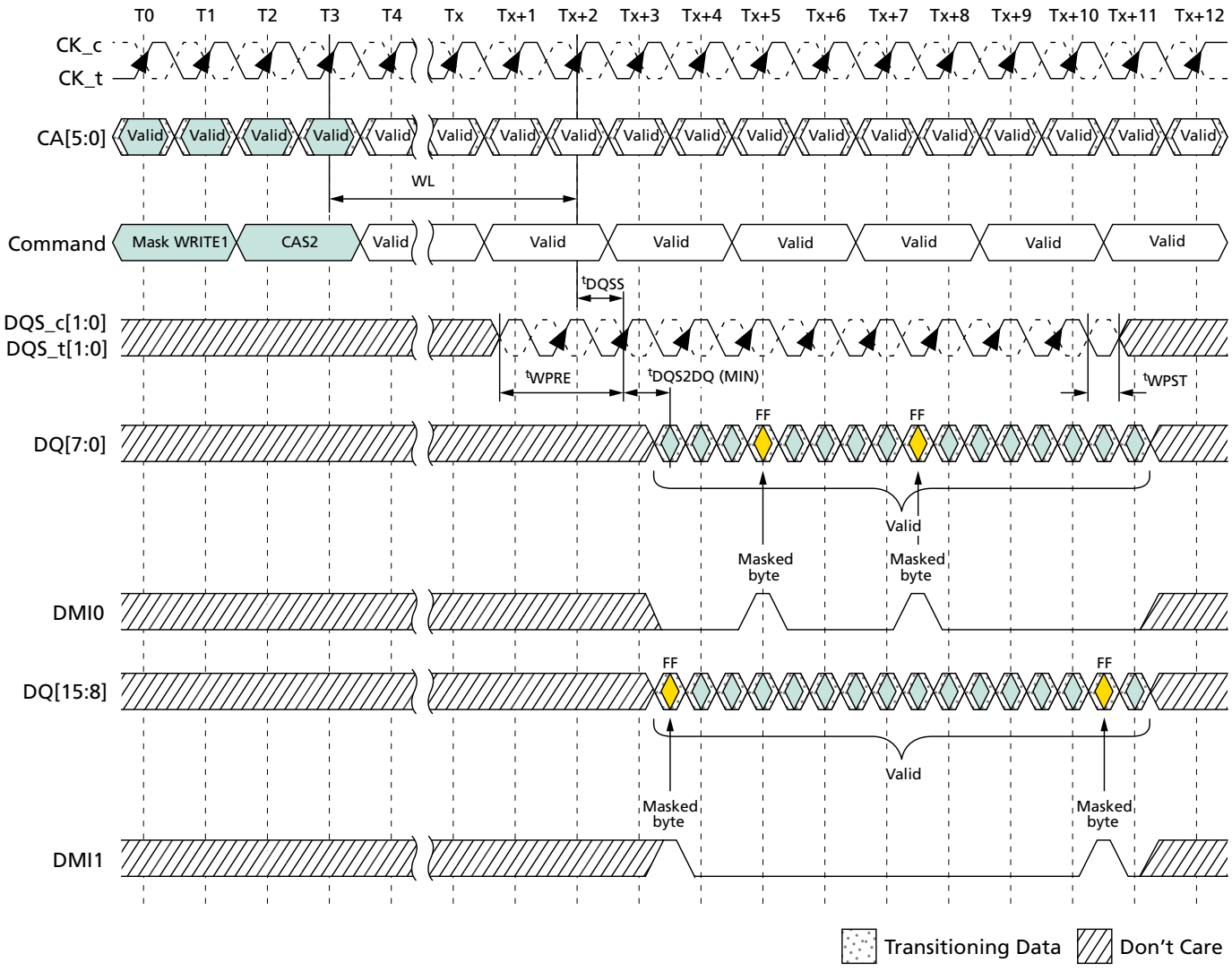
Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(^{t}WTR /^{t}CK)].
2. ^{t} WTR starts at the rising edge of CK after the last latching edge of DQS.

Proposal

MASK WRITE Operation

The LPDDR4-SDRAM requires that WRITE operations that include a byte mask anywhere in the burst sequence must use the MASK WRITE command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The MASK WRITE-1 command is used to begin the operation, followed by a CAS-2 command. A Masked Write command to the same bank cannot be issued until ^{t}CCDMW later, to allow the device to finish the internal READ-MODIFY-WRITE operation. One DATA-MASK-INVERT (DMI) pin is provided per byte lane, and the data-mask-invert timings match data bit (DQ) timing. See Data Mask Invert for more information on the use of the DMI signal.

Figure 16: MASK WRITE Operation – BL16, ^{t}WPRE = 2*n*CK, ^{t}WPST = 0.5*n*CK

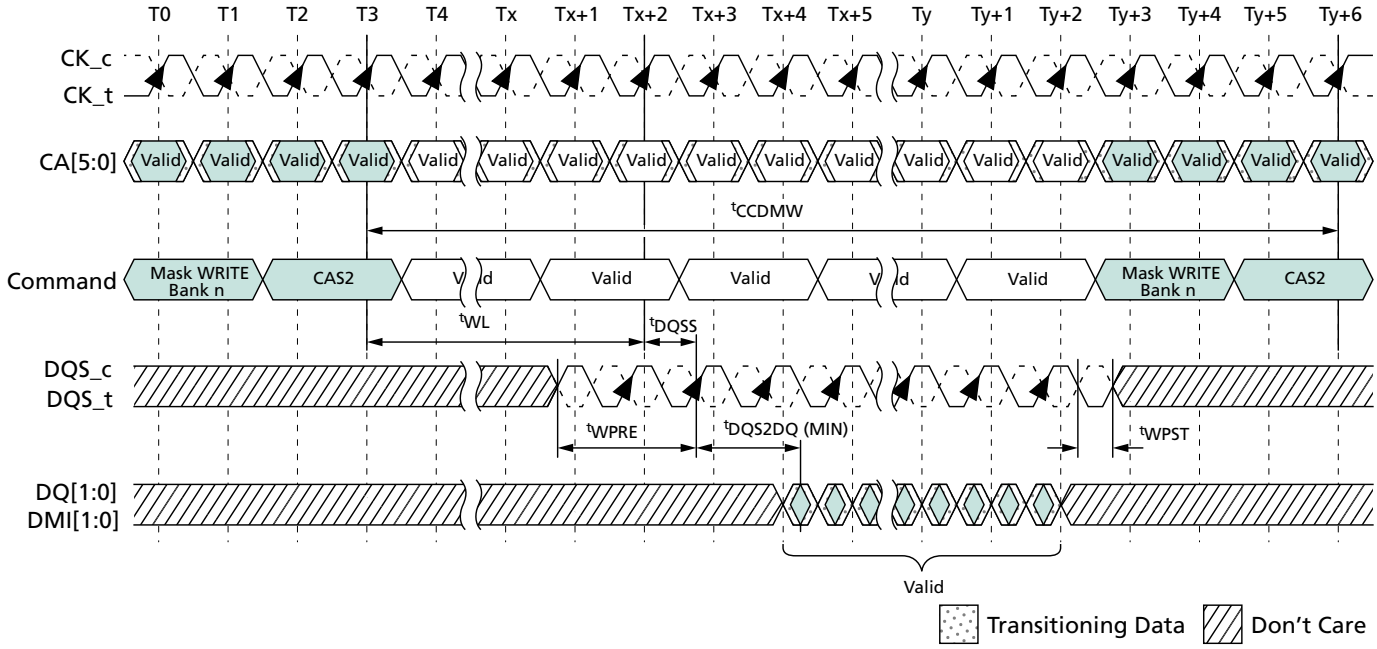


Notes:
1. Mask-write supports only BL16 operations.
2. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

Figure 17: MASK WRITE to MASK WRITE Operation – Same Bank – ^{t}WPRE = 2*n*CK, ^{t}WPST = 0.5*n*CK)

Note:

For BL32 configuration the system needs to insert only 16 bit wide data for masked write operation.



Notes:
1. Mask-write supports only BL16 operations.
2. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.

Proposal

Figure 18: WRITE to MASK WRITE Operation – Same Bank – ^{t}WPRE = 2*n*CK, ^{t}WPST = 0.5*n*CK

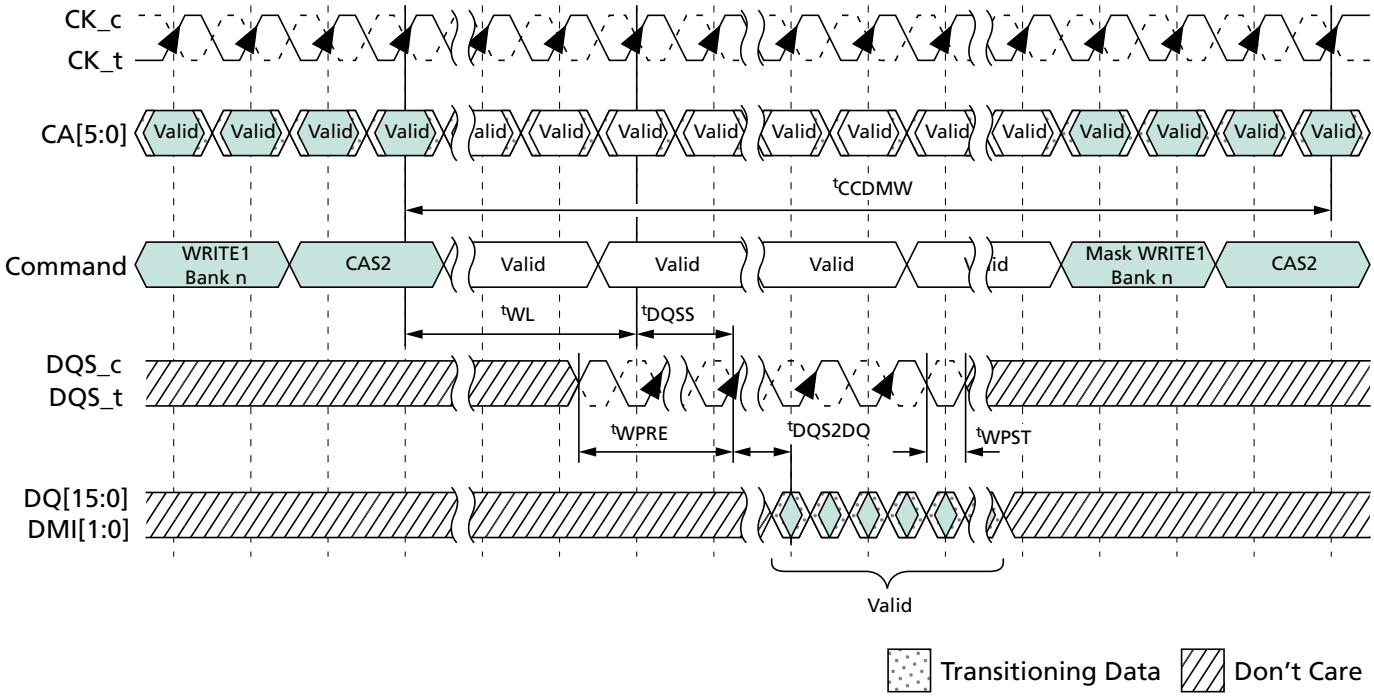
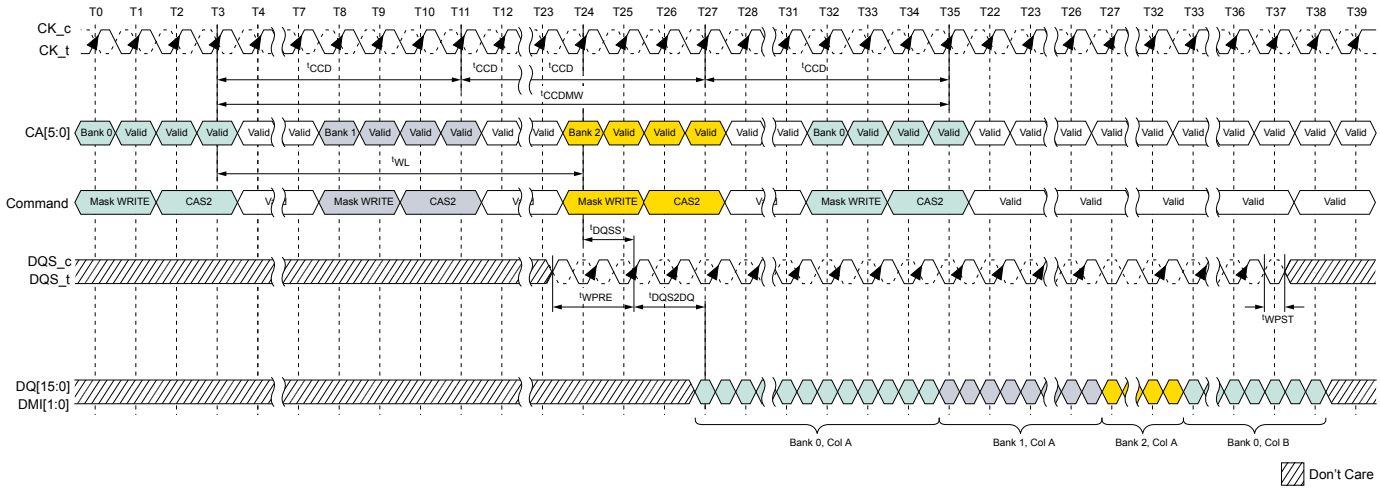


Figure 19: Seamless MASK WRITE Operation – Different Banks



Proposal

Mask Write Timing Constraints for BL16

Table 78: Same Bank

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	illegal	RU(^{t}RCD/^{t}CK)	RU(^{t}RCD/^{t}CK)	RU(^{t}RCD/^{t}CK)	RU(^{t}RAS/^{t}CK)

Table 78: Same Bank (Continued)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
READ (with BL = 16)	illegal	8[1]	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL+ ^{t}WPRE + ^{t}RPST	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	BL/2 + MAX{(8,RU(^{t}RTP/^{t}CK)} - 8
READ (with BL = 32)	illegal	16[2]	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	BL/2 + MAX{(8,RU(^{t}RTP/^{t}CK)} - 8
WRITE (with BL = 16)	illegal	WL + 1+ BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	^{t}CCDMW[3]	WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) + 1
WRITE (with BL = 32)	illegal	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	16[2]	^{t}CCDMW + 8[4]	WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) + 1
MASK WRITE	illegal	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	^{t}CCD	^{t}CCDMW[3]	WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) + 1
PRECHARGE	RU(^{t}RP/^{t}CK), RU(^{t}RPab/^{t}CK)	illegal	illegal	illegal	4

Notes:
1. In the case of BL = 16, ^{t}CCD is 8 × ^{t}CK.
2. In the case of BL = 32, ^{t}CCD is 16 × ^{t}CK.
3. ^{t}CCDMW = 32 × ^{t}CK (4 × ^{t}CCD at BL = 16).
4. WRITE with BL = 32 operation has 8 × ^{t}CK longer than BL =16.

Table 79: Different Bank

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	RU(^{t}RRD/^{t}CK)	4	4	4	4[2]
READ (with BL = 16)	4	8[1]	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL+ ^{t}WPRE + ^{t}RPST	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	4[2]
READ (with BL = 32)	4	16[2]	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + ^{t}RPST	4[2]
WRITE (with BL = 16)	4	WL + 1+ BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	8[1]	4[2]
WRITE (with BL = 32)	4	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	16[2]	16[2]	4[2]
MASK WRITE	4	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	8[1]	4[2]
PRECHARGE	4	4	4	4	4

Notes:
1. In the case of BL = 16, ^{t}CCD is 8 × ^{t}CK.

2. In the case of BL = 32, ^{t}CCD is 16 × ^{t}CK.

PRECHARGE Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CKE, CS, and CA[5:0] in the proper state (see Command Truth Table). The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access ^{t}RPab after an all-bank PRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE command is issued.

To ensure that the device can meet the instantaneous current demands, the row precharge time for an all-bank PRECHARGE (^{t}RPab) is longer than the per-bank precharge time (^{t}RPpb).

Table 80: Precharge Bank Selection

AB (CA[5], R1)	BA2 (CA[2], R2)	BA1 (CA[1], R2)	BA0 (CA[0], R2)	Precharged Bank
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	"Don't Care"	"Don't Care"	"Don't Care"	All banks

Burst Read Operation Followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but the PRECHARGE command cannot be issued until after ^{t}RAS is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (^{t}RP) has elapsed. The minimum read-to-precharge time must also satisfy a minimum analog time from the second rising clock edge of the CAS-2 command. ^{t}RTP begins BL/2 - 8 clock cycles after the READ command.

Figure 20: Burst Read Followed by Precharge – BL16, Toggling Preamble, 0.5*n*CK Postamble

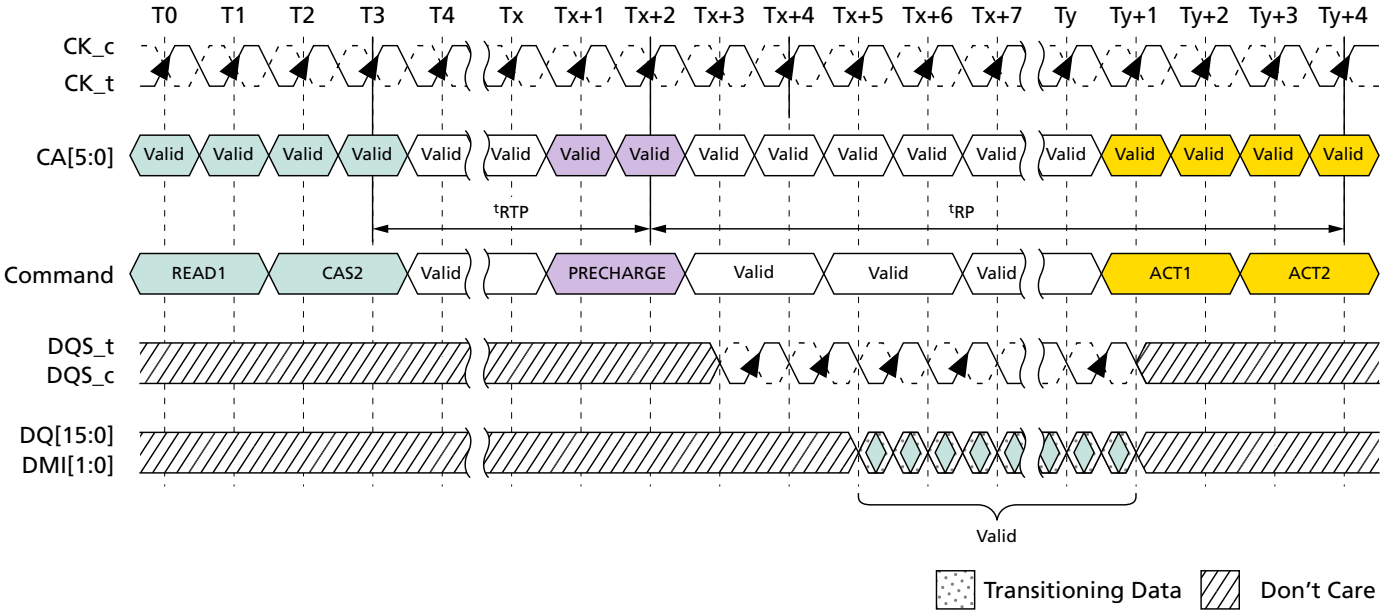
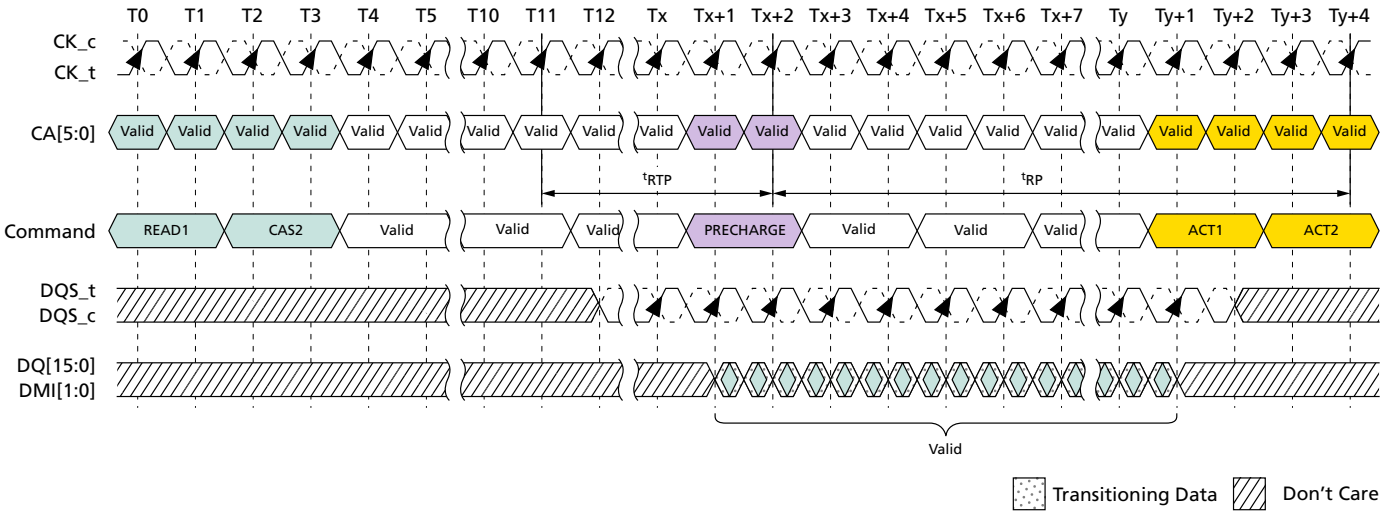


Figure 21: Burst Read Followed by Precharge – BL32, 2^tCK, 0.5*n*CK Postamble



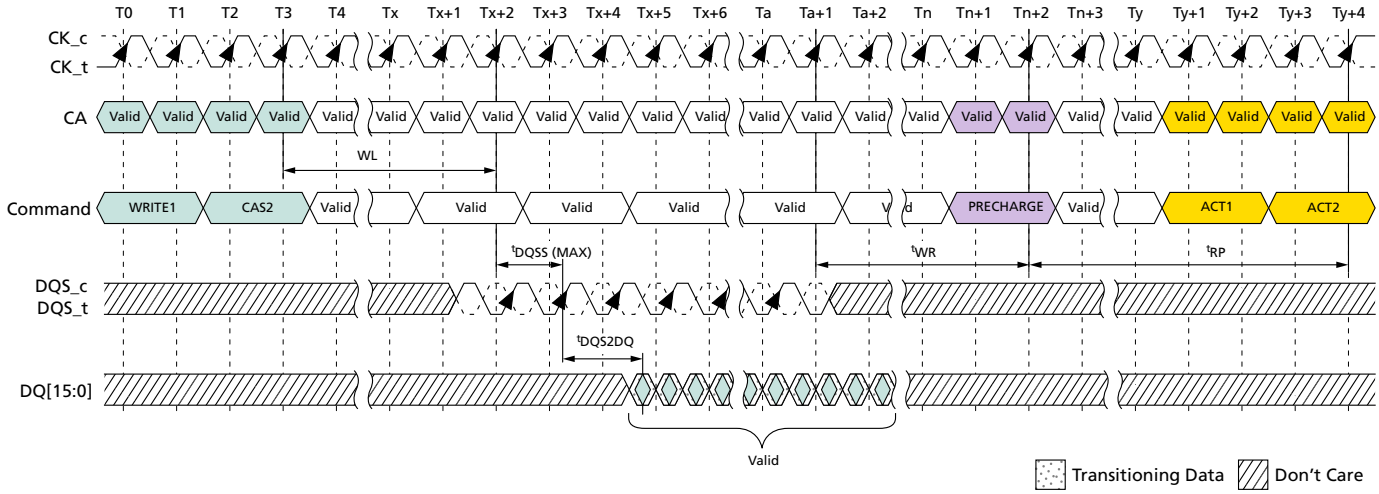
Proposal

Burst Write Followed by Precharge

A write recovery time (^{t}WR) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK after the last valid DQS clock of the burst.

Devices write data to the memory array in prefetch multiples (prefetch = 16). An internal WRITE operation can only begin after a prefetch group has been clocked; therefore, ^{t}WR starts at the prefetch boundaries. The minimum write-to-precharge time for commands to the same bank is WL + BL/2 + 1 + RU(^{t}WR / ^{t}CK) clock cycles.

Figure 22: Burst WRITE Followed by PRECHARGE – BL16, 2*n*CK Preamble, 0.5*n*CK Postamble



Proposal

Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge (AP) function. When a READ or a WRITE command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, the normal READ or WRITE burst operation is executed, and the bank remains active at the completion of the burst.

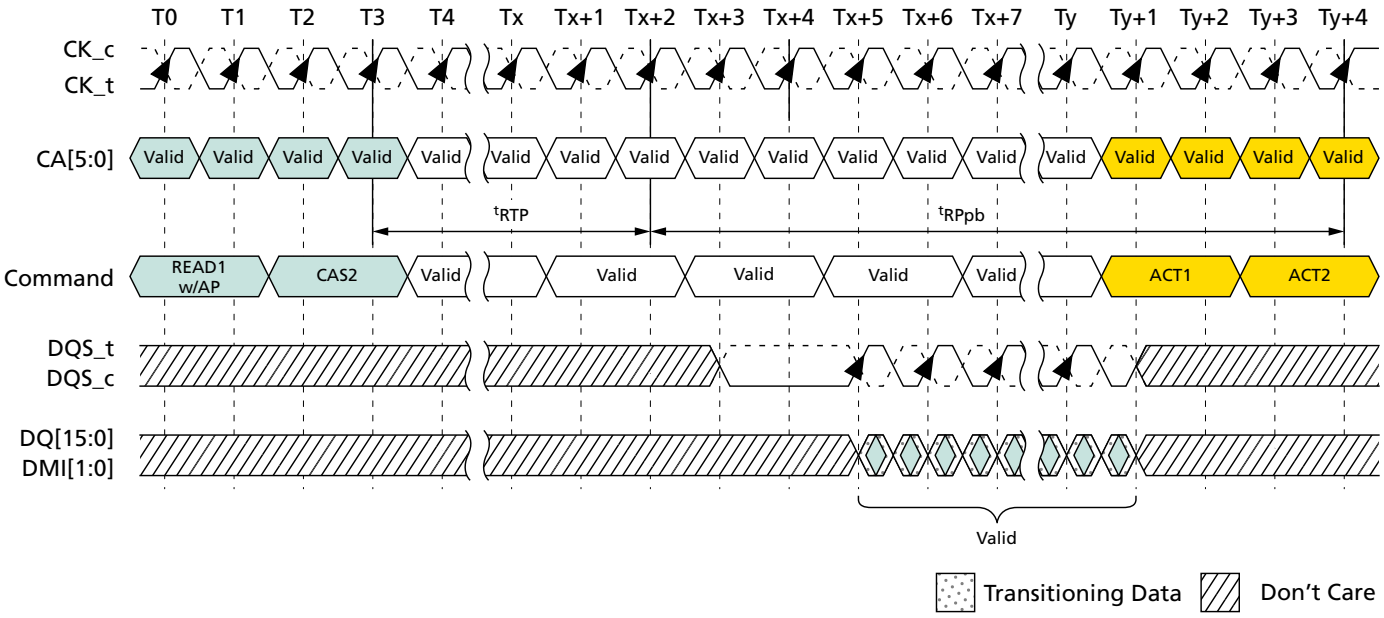
If AP is HIGH when the READ or WRITE command is issued, the auto PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Burst Read With Auto Precharge

If AP is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The devices start an auto precharge operation on the rising edge of the clock at BL/2 after the second beat of the READ w/AP command, or BL/4 - 4 + RU(^{t} RTP /^{t} CK) clock cycles after the second beat of the READ w/AP command, whichever is greater. Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

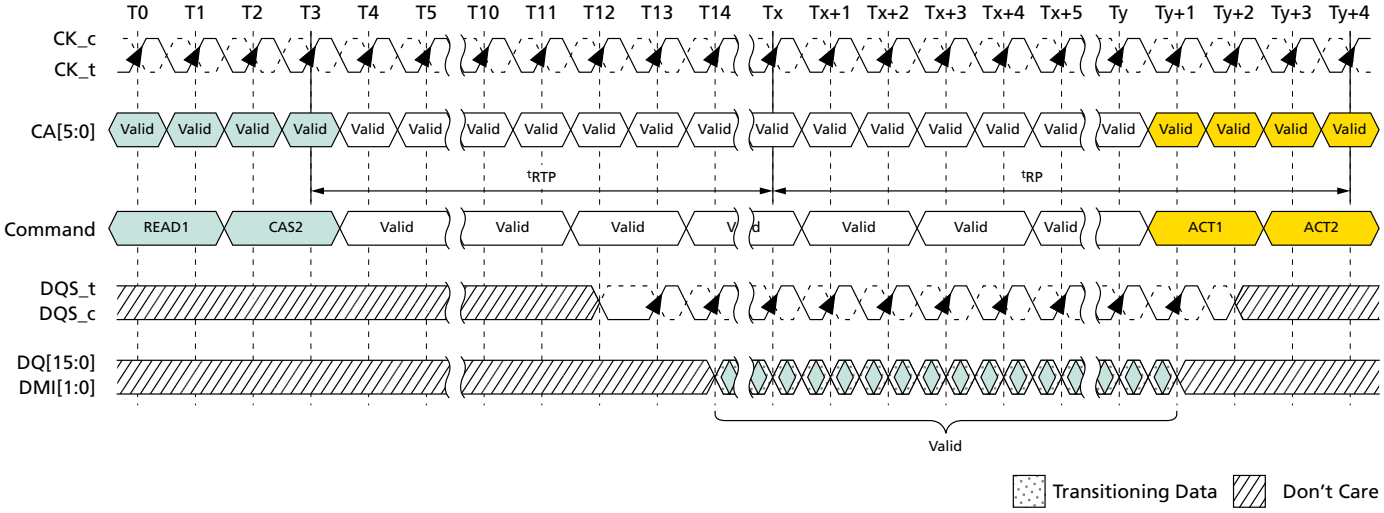
1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 23: Burst ReadWith Auto Precharge – BL16, Non-Toggling Preamble, 0.5*n*CK Postamble



Proposal

Figure 24: Burst Read With Auto Precharge – BL32, Toggling Preamble, 1.5*n*CK Postamble



Burst Write With Auto Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge ^{t}WR cycles after the completion of the burst WRITE.

Following a write with auto precharge, an ACTIVATE command can be issued to the same bank if the following conditions are met:

1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Proposal

Figure 25: Burst Write With Auto Precharge – BL16, 2*n*CK Preamble, 0.5*n*CK Postamble

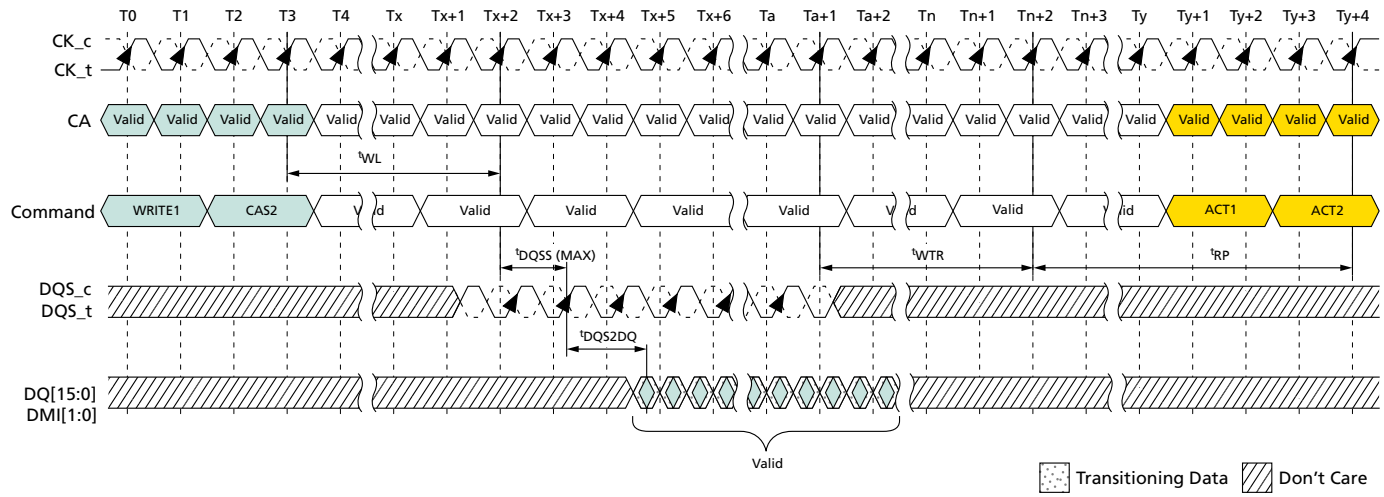


Table 81: Delay Between Commands

From Command	To Command	Minimum Delay Between Commands (^{t}CK)	Notes
READ	PRECHARGE to same bank as READ	BL/2 + MAX(8, RU(^{t}RTP/^{t}CK)) - 8	1
	PRECHARGE ALL	BL/2 + MAX(8, RU(^{t}RTP/^{t}CK)) - 8	1
READ w/AP	PRECHARGE to same bank as READ w/AP	BL/2 + MAX(8, RU(^{t}RTP/^{t}CK)) - 8	1, 2
	PRECHARGE ALL	BL/2 + MAX(8, RU(^{t}RTP/^{t}CK)) - 8	1
	ACTIVATE to same bank as READ w/AP	BL/2 + MAX(8, RU(^{t}RTP/^{t}CK)) - 8	1
	WRITE or WRITE w/AP (same bank)	Illegal	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	
	WRITE or WRITE w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCK/^{t}CK) - WL + WPRE + RPST	3, 4, 5
	MASK-WR or MASK-WR w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCK/^{t}CK) - WL + WPRE + RPST	3, 4, 5
	READ or READ w/AP (same bank)	Illegal	
	READ or READ w/AP (different bank)	BL/2	3
WRITE	PRECHARGE to same bank as WRITE	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	READ w/AP (same bank)	WL + BL/2 + 1 + RU((^{t}WR - ^{t}RTP)/^{t}CK)	
MASK-WR	PRECHARGE (to same bank as MASK-WR)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	READ w/AP (same bank)	WL + BL/2 + 1 + RU((^{t}WR - ^{t}RTP)/^{t}CK)	3

Table 81: Delay Between Commands (Continued)

From Command	To Command	Minimum Delay Between Commands (^{t}CK)	Notes
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	ACTIVATE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RPpb/^{t}CK)	1
	WRITE or WRITE w/AP (same bank)	Illegal	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	
	WRITE or WRITE w/AP (different bank)	BL/2	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	3
	READ or READ w/AP (same bank)	Illegal	
	READ or READ w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	3
MASK-WR w/AP	PRECHARGE (to same bank as MASK-WR w/AP)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	1
	WRITE or WRITE w/AP (same bank)	Illegal	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	
	WRITE or WRITE w/AP (different bank)	BL/2	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	3
	READ or READ w/AP (same bank)	Illegal	
	READ or READ w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	4	1
	PRECHARGE ALL	4	1
PRECHARGE ALL	PRECHARGE	4	1
	PRECHARGE ALL	4	1

Notes:
1. For a given bank, the precharge period should be counted from the latest PRECHARGE command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied ^{t}RP after that latest PRECHARGE command.
2. Any command issued during the minimum delay time as specified in the table above is illegal.

3. After READ w/AP, seamless READ operations to different banks are supported. After WRITE w/AP or MASK-WR w/AP, seamless WRITE operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
4. RPST = 1 if extended postamble is enabled; RPST = 0 if extended postamble is disabled.
5. WPRE = 1 if preamble is 1 × ^{t}CK; WPRE = 2 if preamble is 2 ×^{t}CK.

REFRESH Command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of clock. Per bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. The all-bank REFRESH is initiated with CA5 HIGH at the first rising edge of clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 on the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1, and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. For example, REFpb commands may be issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command, the controller can send another set of per-bank REFRESH commands in the same order or a different order. One possible order can be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. The REFab command also synchronizes the counter between the controller and the device to zero. The device can be placed in self refresh, or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per-bank REFRESH commands in any order, as described above.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD has been satisfied after the prior ACTIVATE command (for example, after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (^{t}RFCpb). However, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- ^{t}RFCpb must be satisfied before issuing a REFab command
- ^{t}RFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}RRD must be satisfied before issuing an ACTIVATE command to a different bank
- ^{t}RFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to every bank in a channel. All banks must be idle when REFab is issued (for example, by issuing a PRE-

CHARGE ALL command prior to issuing an all-bank REFRESH command). The REFab command must not be issued to the device until the following conditions have been met:

- ^{t}RFCab has been satisfied following the prior REFab command
- ^{t}RFCpb has been satisfied following the prior REFpb command
- ^{t}RP has been satisfied following the prior PRECHARGE command

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- RFCab latency must be satisfied before issuing an ACTIVATE command,
- RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 82: REFRESH Command Timing Constraints

Symbol	Minimum Delay From...	To	Notes
^{t}RFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
^{t}RFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed; therefore, REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Figure 26: All-Bank REFRESH Operation

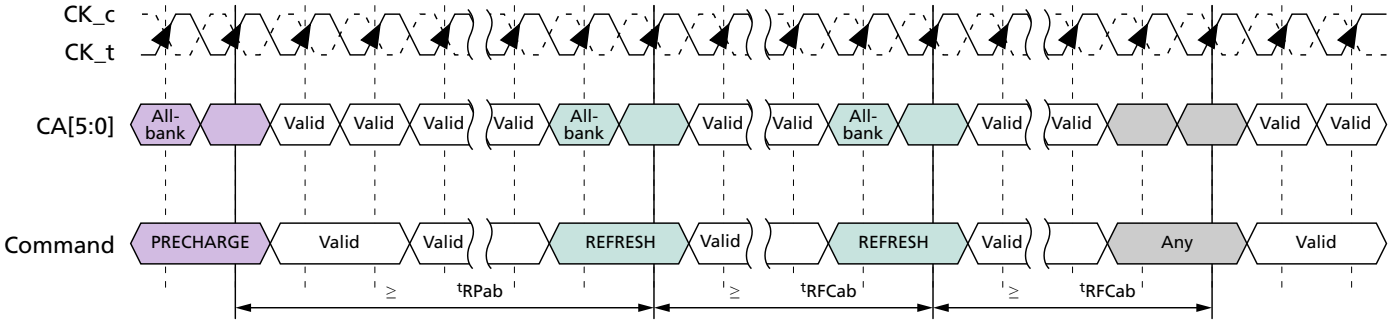
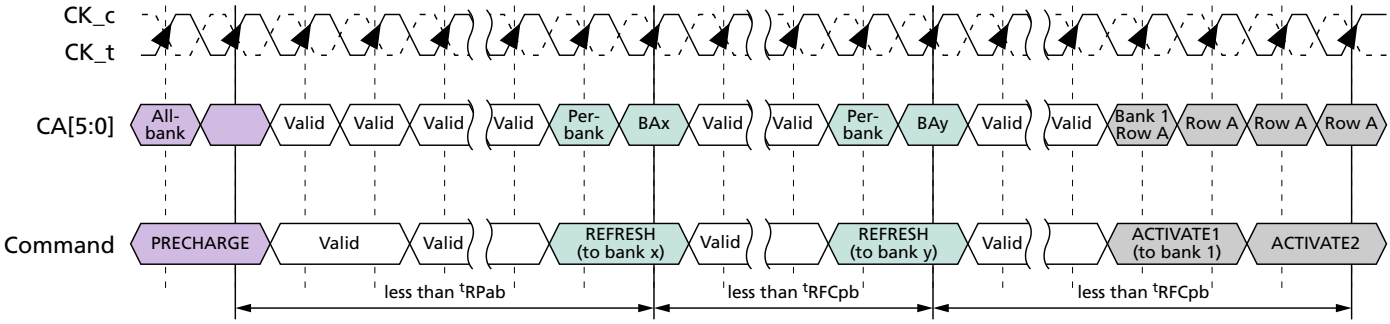


Figure 27: Per-Bank REFRESH Operation



Note: 1. Operations to banks other than the bank being refreshed are supported during the ^{t}RFCpb period.

In general, a REFRESH command needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be postponed during operation of the device, but at no point in time are more than a total of eight REFRESH commands allowed to be postponed. In the case where eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × ^{t}REFI. A maximum of eight additional REFRESH commands can be issued in advance (pulled in), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than eight REFRESH commands in advance does not reduce the number of regular REFRESH commands required later; therefore, the resulting maximum interval between two surrounding REFRESH commands is limited to 9 × ^{t}REFI. At any given time, a maximum of 16 REFRESH commands can be issued within 2 x ^{t}REFI.

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after self refresh) will never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

Figure 28: Postponing REFRESH Commands (Example)

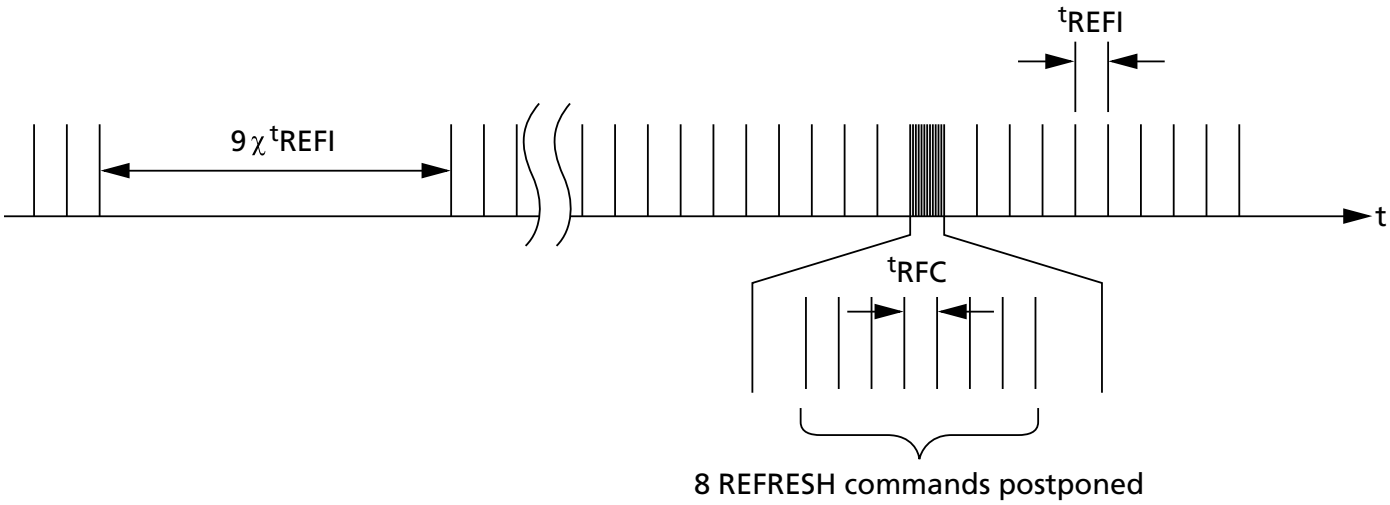
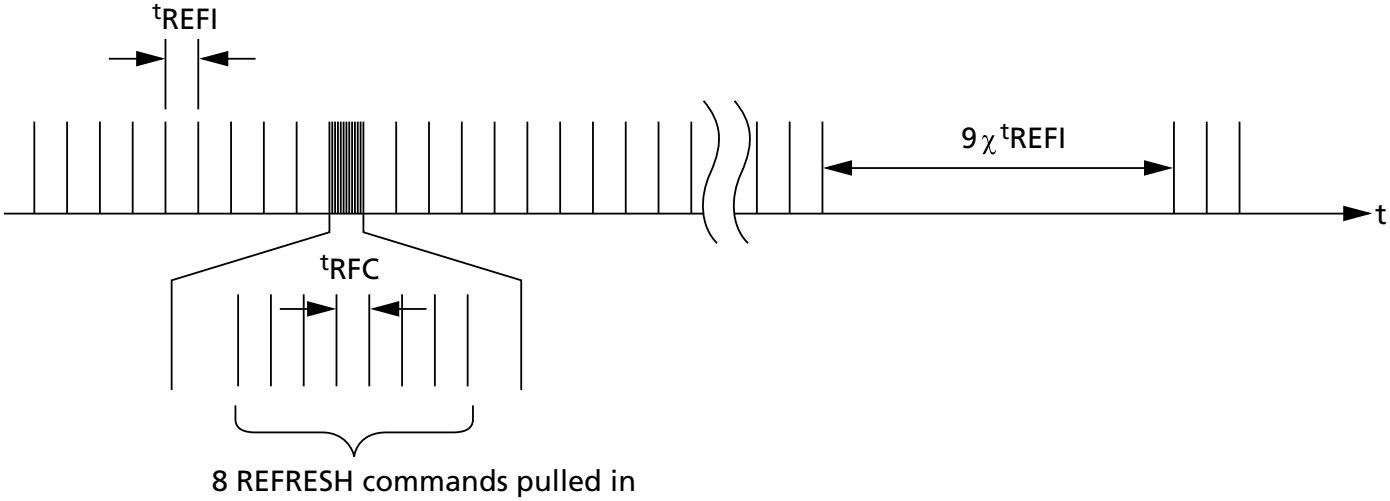


Figure 29: Pulling In REFRESH Commands (Example)



SELF REFRESH Operation

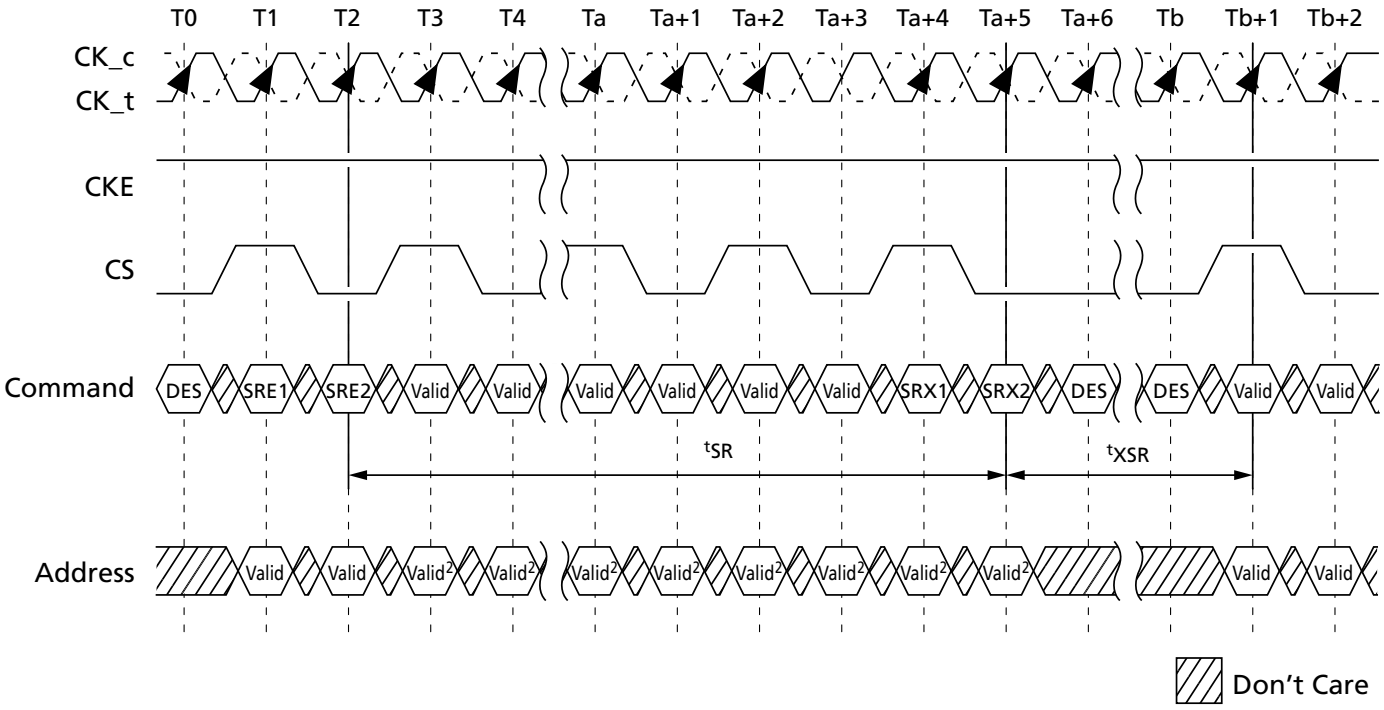
The SELF REFRESH command can be used to retain data in the device without external REFRESH commands. The device has a built-in timer to accommodate SELF REFRESH operation. Self refresh is entered by the SELF REFRESH command defined by having CKE HIGH, CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH, CA4 HIGH, and CA5 valid (valid meaning that it is at a logic level HIGH or LOW) for the first rising edge, and CKE HIGH, CS LOW, CA0 valid, CA1 valid, CA2 valid, CA3 valid CA4 valid, and CA5 valid at the second rising edge of clock. The SELF REFRESH command is only allowed when the device is in the idle state.

During self refresh mode, external clock input is needed and all input pins of the device are activated. The device can accept the following commands: MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2, except PASR bank/segment setting.

The device can operate in self refresh mode within the standard and extended temperature ranges. It also manages self refresh power consumption when the operating temperature changes: lower at low temperatures and higher at high temperatures.

For proper SELF REFRESH operation, power supply pins (V_{DD1}, V_{DD2}) must be at valid levels. V_{DDQ} can be turned off after ^{t}ESCKE is satisfied. Prior to exiting self refresh, V_{DDQ} must be within specified limits. The minimum time that the device must remain in self refresh mode is ^{t}SR (MIN).

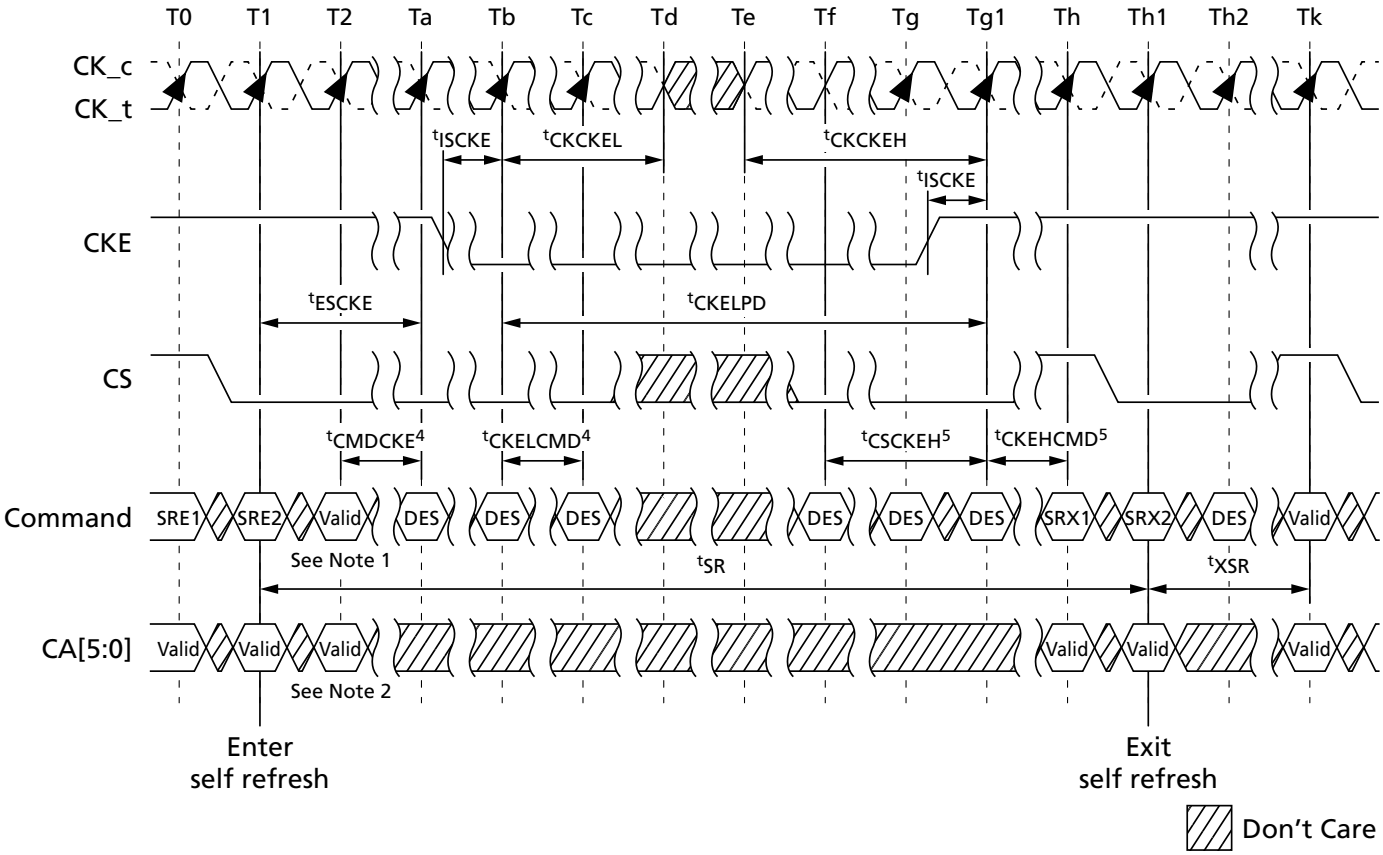
Figure 30: Self Refresh Entry/Exit Timing



Notes:
1. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. Address inputs can be "Don't Care" (but valid) during a DESELECT command.

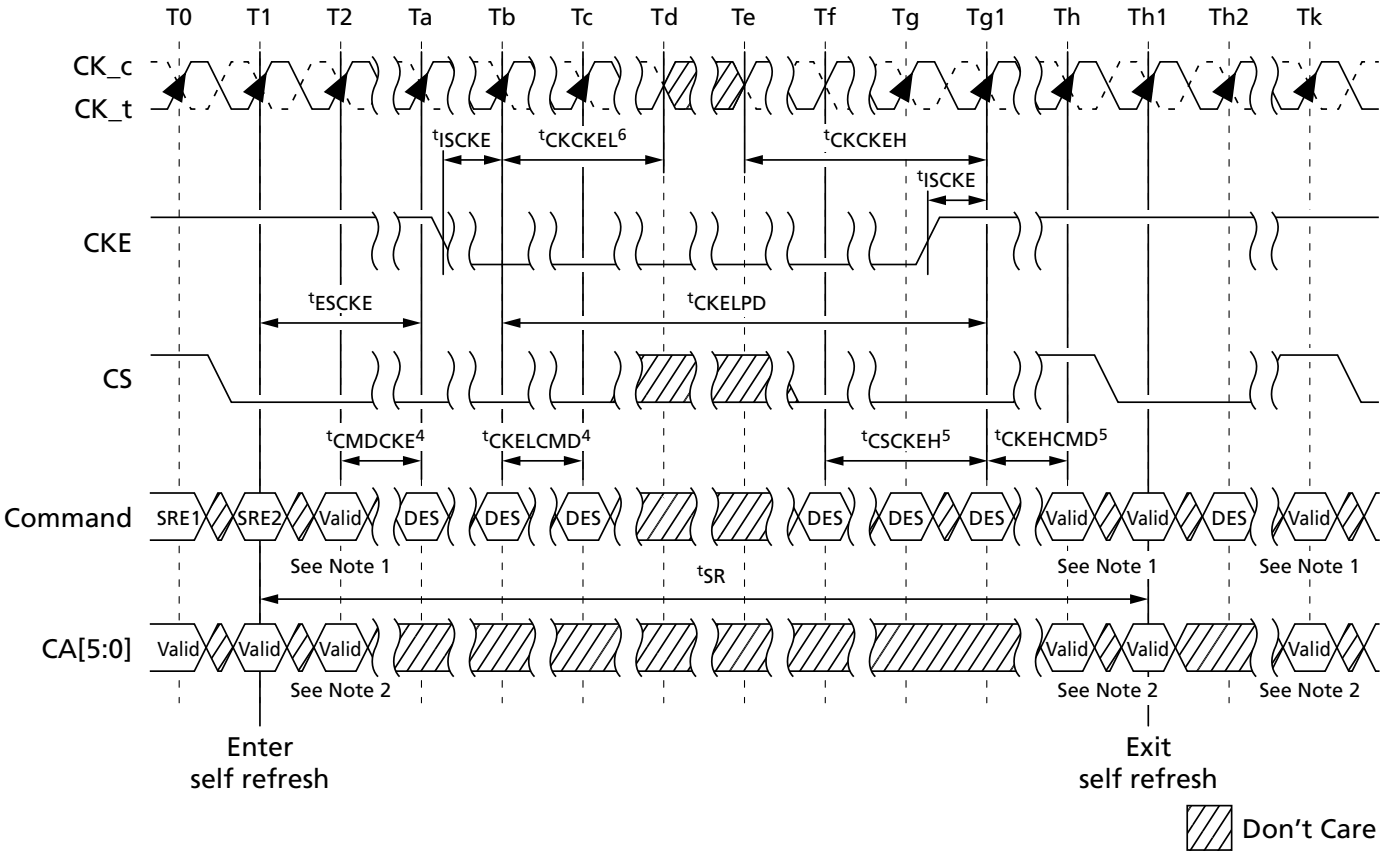
Entering/exiting power-down mode is allowed during self refresh mode. The related timing parameters between self refresh entry/exit and power-down entry/exit are shown below.

Figure 31: Power-Down Entry and Exit During Self Refresh



Notes:
1. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. Address inputs can be "Don't Care" (but valid) during a DESELECT command.
3. CS input must be LOW during a DESELECT command.
4. Deselect is only allowed during ^{t}CMDCKE (MIN) and ^{t}CKELCMD (MIN).
5. Deselect is only allowed during ^{t}CSCKEH (MIN) and ^{t}CKEHCMD (MIN).
6. The input clock frequency can be changed after ^{t}CKCKEL (MIN) is satisfied.

Figure 32: Command Input Timing After Power-Down Exit



Notes:
1. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. Address inputs can be "Don't Care" (but valid) during a DESELECT command.
3. CS input must be LOW during a DESELECT command.
4. Deselect is only allowed during ^{t}CMDCKE (MIN) and ^{t}CKELCMD (MIN).
5. Deselect is only allowed during ^{t}CSCKEH (MIN) and ^{t}CKEHCMD (MIN).
6. The input clock frequency can be changed after ^{t}CKCKEL (MIN) is satisfied.

Table 83: Self Refresh Timing Parameters

Speed		LPDDR4-3200		LPDDR4-4266			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CKE input setup time	^{t}ISCKE	TBD	-	TBD	-		
Valid clock requirement after CKE Input LOW	^{t}CKCKEL	MAX (7.5ns, 3 ^{t}CK)	-	MAX (7.5ns, 3 ^{t}CK)	–	nCK	

Table 83: Self Refresh Timing Parameters (Continued)

Speed		LPDDR4-3200		LPDDR4-4266			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Valid clock requirement after CKE input HIGH	tCKCKEH	2 tCK	-	2 tCK	–	nCK	
Delay from SRE command to CKE LOW	tESCKE	2	-	2	–	nCK	
Delay from valid command to CKE input LOW	tCMDCKE	2	-	2	-	nCK	
CKE minimum pulse width	tCKELPD	MAX (7.5ns, 3 tCK)	–	MAX (7.5ns, 3 tCK)	–	nCK	
Valid command requirement after CKE input LOW	tCKELCMD	MAX (7.5ns, 3 tCK)	–	MAX (7.5ns, 3 tCK)		nCK	
Valid command requirement after CKE input HIGH	tCKEHCMD	MAX (7.5ns, 3 tCK)	–	MAX (7.5ns, 3 tCK)	–	nCK	
Valid CS LOW requirement before CKE input HIGH	tCSCKEH	TBD	–	TBD	–	nCK	
Minimum self refresh time	tSR	TBD		TBD	–	nCK	
Exit self refresh to valid commands	tXSR	MAX (tRFCab + 7.5ns, 2nCK)	–	MAX (tRFCab + 7.5ns, 2nCK)	–	nCK	1

Note: 1. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

Self Refresh Abort

If MR:x bit :y is enabled, the device aborts any ongoing refresh during self refresh exit and does not increment the internal refresh counter. The controller can issue a valid command after a delay of tXSR_abort instead of tXSR.

The value of tXSR_abort (MIN) is defined as tRFCpb + 10ns.

Upon exit from self refresh mode, the device requires a minimum of one extra refresh (eight per bank or one for the entire bank) before entering a subsequent self refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

Self refresh abort is valid for 16Gb and larger densities only.

MODE REGISTER READ Operation

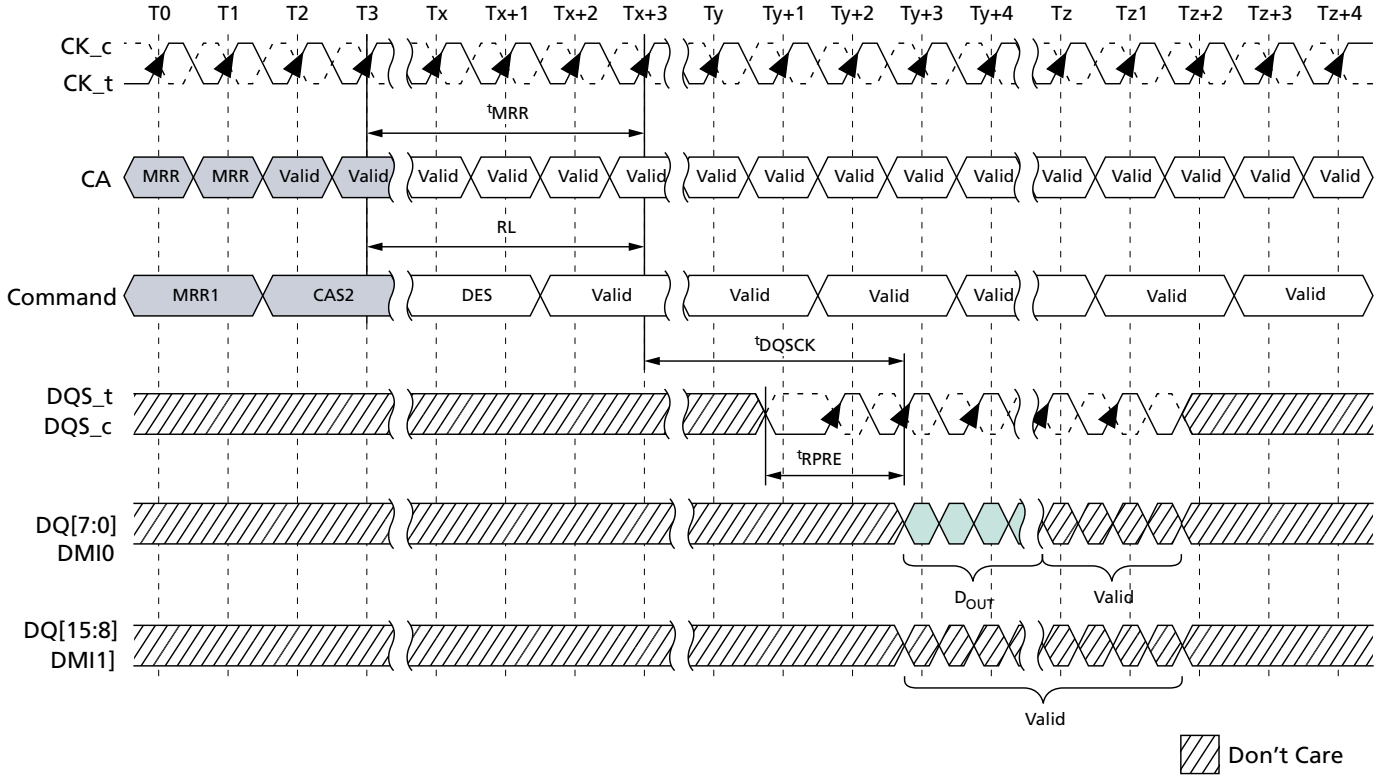
The MODE REGISTER READ (MRR) command is used to read configuration and status data from the device registers. The MRR command is initiated with CKE, CS, and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) enable the user to select one of 64 registers. The mode register contents are available on the first UI data bits of DQ[7:0] after RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ following the MRR command. Subsequent data beats contain valid but undefined content. DQS is toggled for the duration of the mode register read burst. The MRR has a command burst length of 16. MRR operation must not be interrupted.

Table 84: MRR

BL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0				V											
DQ1	OP1				V											
DQ2	OP2				V											
DQ3	OP3				V											
DQ4	OP4				V											
DQ5	OP5				V											
DQ6	OP6				V											
DQ7	OP7				V											
DBIO	V															

Notes:
1. MRR data are extended to the first 4 UIs, allowing the LPDRAM controller to sample data easily.
2. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be LOW.
3. The read pre-amble and post-amble of MRR are the same as for a normal read.

Figure 33: MODE REGISTER READ Operation



Notes:
1. Only BL=16 is supported.
2. Only DESELECT is allowed during tMRR period.

Proposal

MRR Following Idle Power-Down State or SREF Power-Down

Following the idle power-down state or a power-down state within self refresh, an additional time, tMMRI , is required prior to issuing the MRR command. This additional time (equivalent to tRCD) is required in order to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) writes configuration data to the mode registers. The MRW command is initiated with CKE, CS, and CA[5:0] to valid levels at the rising edge of the clock. The mode register address and the data written to it is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.

Figure 34: MODE REGISTER WRITE Timing

Mode Register Write States

MRW can be issued from either a bank-idle or a bank-active state. Certain restrictions may apply for MRW from an active state.

Table 85: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
Bank(s) active	MRR	Reading mode register	Bank(s) active
	MRW	Writing mode register	Bank(s) active

Command Bus Training Mode

The command bus must be trained before enabling termination for high-frequency operation. The device provides an internal $V_{REF(CA)}$ that defaults to a level suitable for unterminated, low-frequency operation, but the $V_{REF(CA)}$ must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation.

The training mode described here centers the internal $V_{REF(CA)}$ in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the CA bus training mode.

The die has a bond-pad (ODT_CA) to control the command bus termination for multi-rank operation. Other mode register bits are provided to fine tune termination control in a variety of system configuration. See On Die Termination for more information.

The device uses frequency set points to enable multiple operating settings for the die. The device defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the termination should be enabled for one die in each channel by setting MR13 OP[6] = 1b (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Upon training entry, the device will automatically switch to FSP-OP[1] and use the high-frequency settings during training (See the Command Bus Training Entry Timing figure for more information on FSP-OP register sets). Upon training exit, the device will automatically switch back to FSP-OP[0], returning to a "known-good" state for unterminated, low-frequency operation.

To enter command bus training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0] = 1b (command bus training mode enabled). After time ^{t}MRD , CKE may be set LOW, causing the device to switch to FSP-OP[1], and completing the entry into command bus training mode.

At time ^{t}CAENT later, the $V_{REF(CA)}$ value may be changed by presenting the $V_{REF(CA)}$ range (as defined by MR12-OP[6]) onto DQ[6] and the $V_{REF(CA)}$ value (as defined by MR12-OP[5:0]) onto DQ[5:0] and toggling DQS at least one full cycle. When latching the $V_{REF(CA)}$ range and value, DQS may toggle up to the number of times found in a burst

length 16 (BL16) transfer, including preamble and postamble toggles. The new $V_{REF(CA)}$ value must "settle" for time ^{t}VREF_LONG before attempting to latch CA information.

Note: If DQ-ODT is enabled in MR11-OP[2:0], then the SDRAM will terminate the DQ lanes during command bus training when entering $V_{REF(CA)}$ range and values on DQ[6:0].

To verify that the receiver has the correct $V_{REF(CA)}$ setting, and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

To start, if the relationship of CS relative to CK is unknown, CS may be trained by presenting a short (UI) CS pulse with a long CA pulse (nUI). Next, check the Rx latch results on the DQ bus, and then move CS relative to CK and repeat until CS is centered on the latching edge of CK. Once CS is trained, the CA signals may be trained by sending short (UI) CA pulses of varying data, checking the Rx latch results on the DQ bus, and then moving CA relative to CK and repeating until CA is centered on the latching edge of CK. Any combination of $V_{REF(CA)}$, CS, and CA alignment can be trained using this simple training mode. See the timing diagrams below and AC Timing further timing constraints in the command bus training mode.

To exit command bus training mode, drive CKE HIGH, and after time ^{t}VREF_LONG, issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0] = 0b. After time ^{t}MRW, the device is ready for normal operation. After training exit, the device will automatically switch back to the FSP-OP registers that were in use prior to training.

Training Sequence for Single-Rank Systems

The sequence example shown here assumes an initial low-frequency operating point training a high-frequency operating point. The bold text shows high-frequency instructions. Any operating point may be trained from any known good operating point.

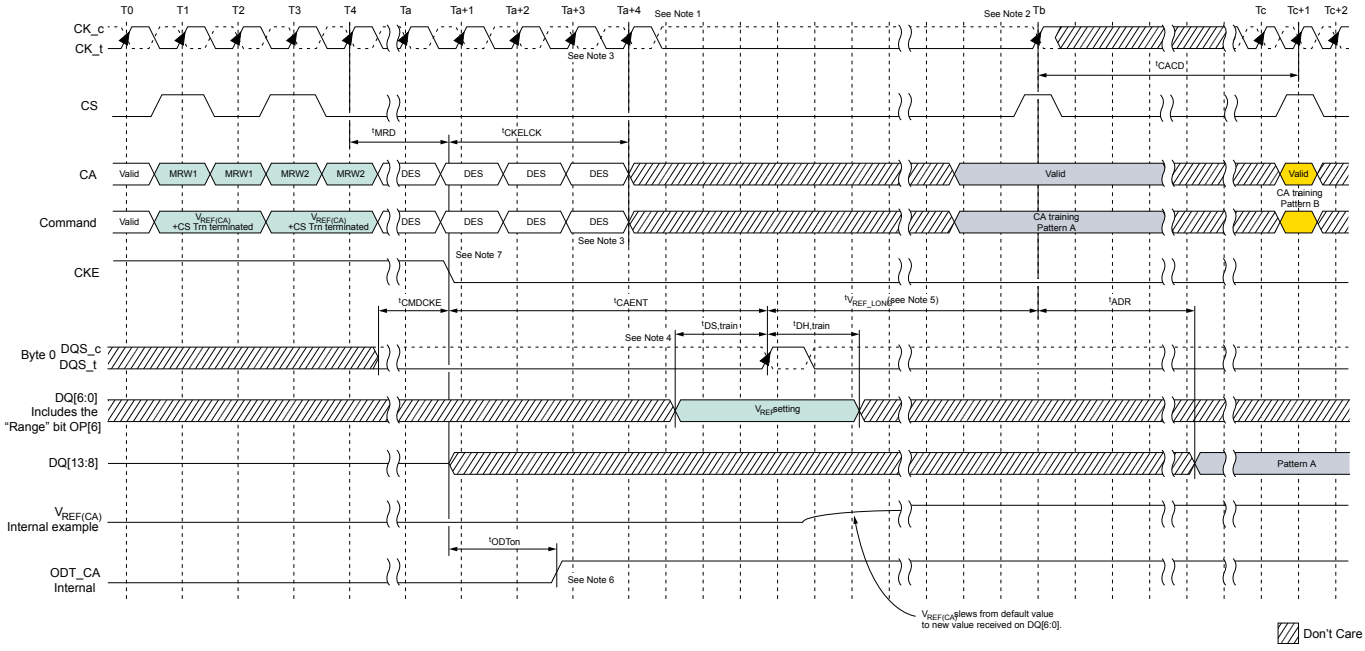
1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-OP[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter command bus training mode.
4. Drive CKE LOW, **and change CK frequency to the high-frequency operating point.**
5. **Perform command bus training ($V_{REF(CA)}$, CS, and CA).**
6. **Exit training by driving CKE HIGH,** change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained).
7. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point. At this point the command bus is trained and you may proceed to other training or normal operation.**

Training Sequence for Multiple-Rank Systems

The sequence example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The bold text shows high-frequency instructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-WR[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels and ranks to set up high-frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7] = 1b.
4. Issue MRW-1 and MRW-2 commands to enter command bus training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), **and change CK frequency to the high-frequency operating point.**
6. **Perform command bus training on the terminating rank ($V_{REF(CA)}$, CS, and CA).**
7. **Exit training by driving CKE HIGH,** change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[1] (or FSP-WR[0]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained by the device).
8. Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminating rank (but keep CKE HIGH).
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point.**
10. **Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[1] (or FSP-OP[0]).**
11. **Perform command bus training on the non-terminating rank ($V_{REF(CA)}$, CS, and CA).**
12. **Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[0] (or FSP-OP[1]) to turn off termination.**
13. **Exit training by driving CKE HIGH on the non-terminating rank,** change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the device).
14. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point. At this point the command bus is trained for both ranks and the user may proceed to other training or normal operation.**

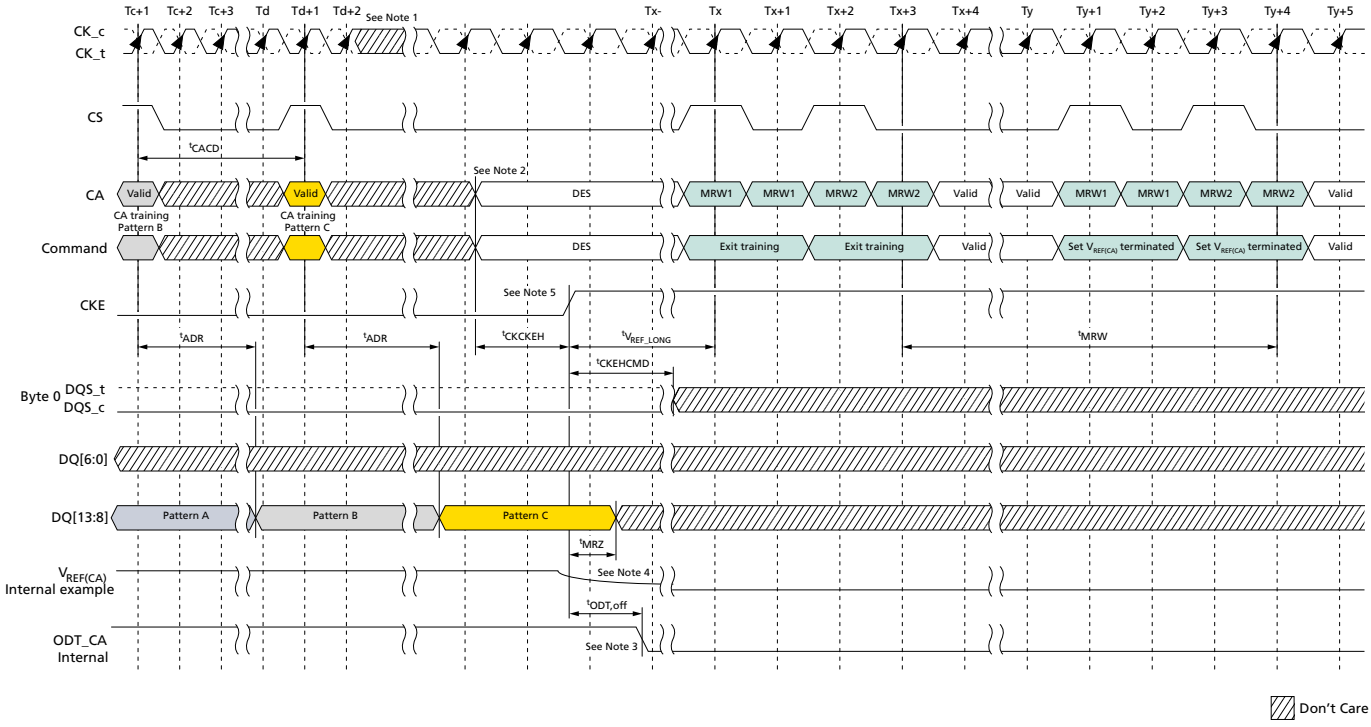
Figure 35: Command Bus Training Entry Timing



Notes:
1. After tCKELCK, the clock can be stopped or the frequency changed any time.
2. Only one CK edge is necessary to latch CS and CA states during training. However, a stable clock prior to sampling is required to ensure timing accuracy.
3. Continue to drive CK, and hold CA and CS LOW, until tCKELCK after CKE is LOW (which disables command decoding).
4. DQS_t[0], DQS_c[0] may pulse as many times as needed to latch the V_{REF} setting on DQ[6:0]. The value of the DQ[6:0] pins that meets tDS,train/ tDH,train from the last DQS pulse will be valid tVREF_LONG later. The DQS pins should not pulse during the tVREF_LONG time.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new V_{REF} setting is a single step above or below the old V_{REF} setting; 2) The DQS pulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets tDS,train/ tDH,train for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (non-active) set. For example, if the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering command bus training to ensure that ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values. If the alternate FSP-OP has ODT_CA disabled, then termination will not be enabled in command bus training mode. If the ODT_CA pad is bonded to V_{SS} or floating, ODT_CA termination will never enable for that die.
7. When CKE is driven LOW in command bus training mode, the device will change operation to the alternate FSP, i.e., the inverse of the FSP programmed in the FSP-OP mode register.

Proposal

Figure 36: Command Bus Training Exit Timing



Notes:
1. The clock can be stopped or the frequency changed any time before ^{t}CKCKEH. CK must meet ^{t}CKCKEH before CKE is driven HIGH. When CKE is driven HIGH, the clock frequency must be returned to the original frequency (i.e., the frequency corresponding to the FSP at command bus training mode entry.
2. CS and CA[5:0] must be deselected (LOW) ^{t}CKCKEH before CKE is driven HIGH.
3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP prior to command bus training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]). For example, if the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device and must be written to the FSP-OP register set before returning to operation at the trained frequency. For example, $V_{REF(CA)}$ will return to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bus training mode entry.

Table 86: Command Bus Training Timing Parameters

Parameter	Symbol	Min/ Max	Value	Units	Notes
Clock and command valid after CKE LOW	^{t}CKELCK	Min	MAX (7.5ns, 3nCK)	^{t}CK	
		Max	–		
Clock and command valid before CKE HIGH	^{t}CKCKEH	Min	2	^{t}CK	
		Max	–		
Data setup for V_{REF} training mode	^{t}DS,train	Min	2	ns	
		Max	–		

Table 86: Command Bus Training Timing Parameters (Continued)

Parameter	Symbol	Min/ Max	Value	Units	Notes
Data hold for V_{REF} training mode	^{t}DH,train	Min	2	ns	
		Max	–		
Asynchronous data read	^{t}ADR	Min	–	ns	
		Max	20		
CA BUS TRAINING command to CA BUS TRAINING command delay	^{t}CACD	Min	RU (^{t}ADR + 2nCK)	^{t}CK	1, 2
		Max	–		
First CA BUS TRAINING command following CKE LOW	^{t}CAENT	Min	10	ns	
		Max	–		
CA bus training CKE HIGH to DQ tri-state	^{t}MRZ	Min	1.5	ns	
		Max	-		
MODE REGISTER WRITE SET command delay	^{t}MRD	Min	MAX (14ns, 10nCK)	ns	
		Max	–		
V_{REF} step time – multiple steps	^{t}VREF_LONG	Min	200	ns	
		Max	–		
V_{REF} step time – one step	^{t}VREF_SHORT	Min	80	ns	
		Max	–		

Notes:
1. If ^{t}CACD is violated, the data for samples which violate ^{t}CACD will not be available, except for the last sample (where ^{t}CACD after this sample is met). Valid data for the last sample will be available after ^{t}ADR.
2. DQ[15:14] shall be driven to a valid level ("Don't Care") by the device during command bus training.

MULTIPURPOSE Operation

The device uses the MULTIPURPOSE (MPC-1) command to issue a NO OPERATION (NOP) command and to access various training modes. The MPC-1 command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC-1 command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC-1 command. When OP[6] = 0, the device executes a NOP command, and when OP[6] = 1, the device further decodes one of several training commands.

When OP[6] = 1 and the training command includes a READ or WRITE operation, the MPC-1 command must be followed immediately by a CAS-2 command. For training commands that read or write, READ latency (RL) and WRITE latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as a typical READ or WRITE command. The operands of the CAS-2 command following a MPC READ/WRITE command must be driven LOW. The following MPC commands must be followed by a CAS-2 command:

- WRITE FIFO
- READ FIFO
- READ DQ CALIBRATION

All other MPC commands do not require a CAS-2 command, including the following:

- NOP
- START DQS INTERVAL OSCILLATOR
- STOP DQS INTERVAL OSCILLATOR
- START ZQ CALIBRATION
- LATCH ZQ CALIBRATION

Table 87: MPC Command Definition

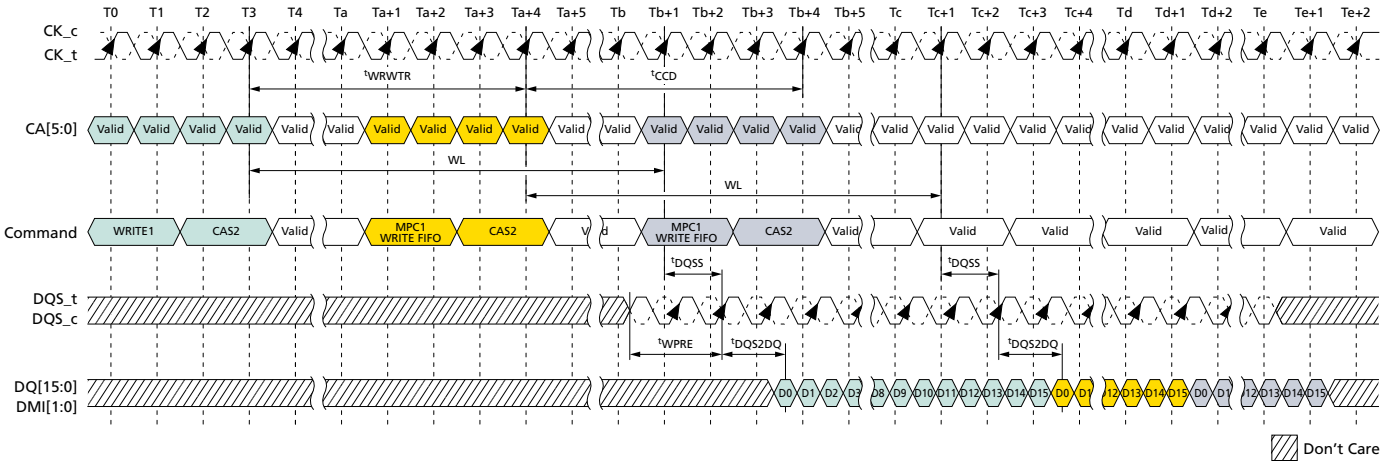
SDR Command	SDR Command Pins			SDR CA Pins						CK_t Edge	Notes
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5		
	CK_t (n-1)	CK_t(n)									
MPC-1 (Train, NOP)	H	H	H	L	L	L	L	L	OP6	↑1	1, 2
			L	OP0	OP1	OP2	OP3	OP4	OP5	↑2	

Notes:
1. See the Command Truth Table for more information.
2. MPC-1 commands for READ or WRITE training operations must be immediately followed by the CAS-2 command, consecutively, without any other commands in between. The MPC-1 command must be issued before issuing the CAS-2 command.

Table 88: MPC Commands

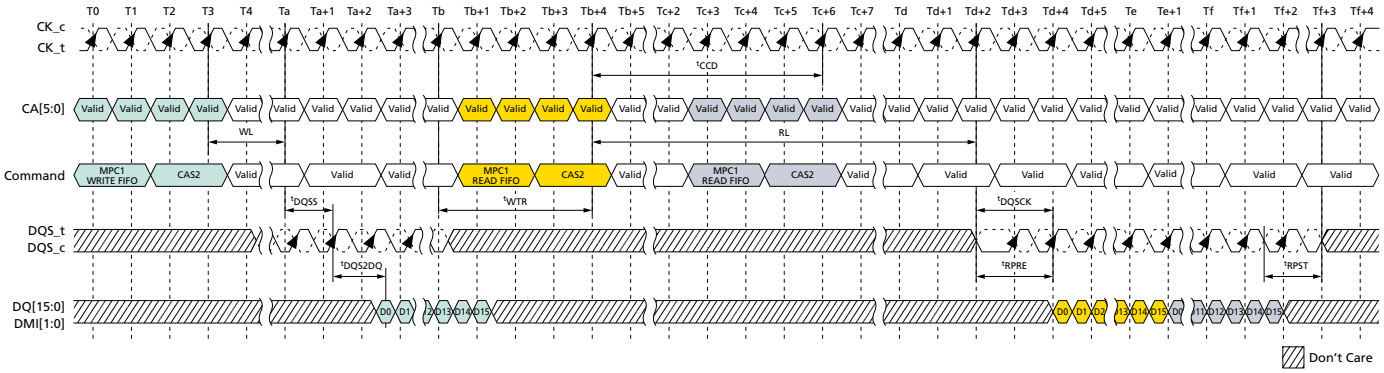
Function	Operand	Data
Training Modes	OP[6:0]	**0XXXXXXb:** NOP
		1000001b: Read FIFO
		1000011b: Read DQ Calibration (MR32/MR40)
		1000101b: RFU
		1000111b: Write FIFO
		1001011b: Start DQS Oscillator
		1001101b: Stop DQS Oscillator
		1001111b: ZQCal Start
		1010001b: ZQCal Latch
		All Others: Reserved

Figure 37: MPC-1 (WR-FIFO) Operation – ^{t}WPRE = 2nCK, ^{t}WPST = 0.5nCK



Notes:
1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh, with CKE HIGH.
2. Write-1 to MPC-1 is shown as an example of command-to-command timing for MPC-1. Timing from write-1 to MPC-1 [WR-FIFO] is ^{t}WRWTR.
3. Seamless MPC-1 [WR-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC-1 [WR-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS, ^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of 5 MPC-1 [WR-FIFO] commands may be executed consecutively without corrupting FIFO data. The 6th MPC-1 [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC-1 [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other commands in between. See Write Training for more information on FIFO pointer behavior.

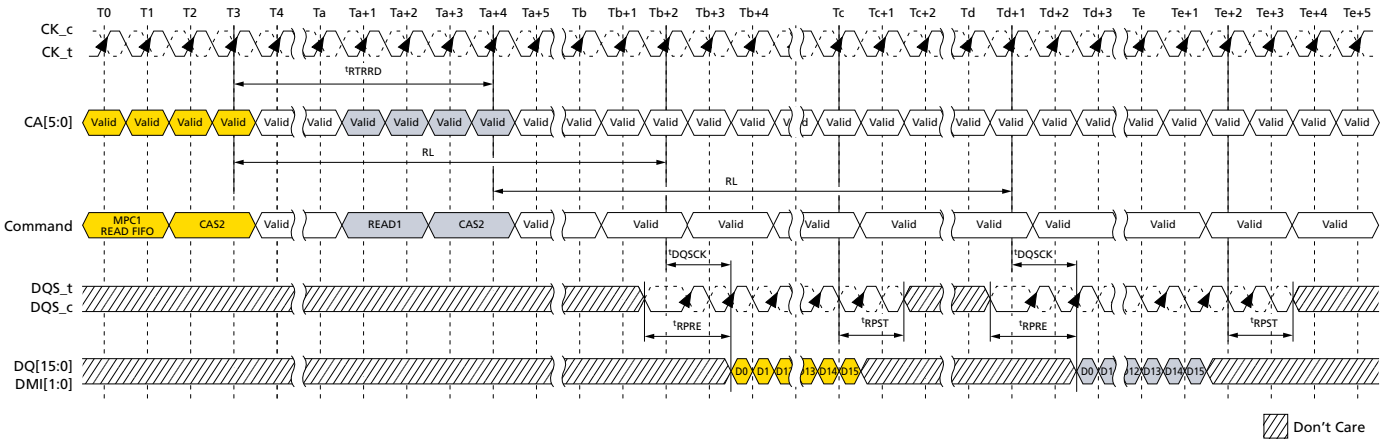
Figure 38: MPC-1 [RD-FIFO] Operation – ^{t}WPRE = 2nCK, ^{t}WPST = 0.5nCK, ^{t}RPRE = Toggling, ^{t}RPST = 1.5nCK



Notes:

1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. MPC-1 [WR-FIFO] to MPC-1 [RD-FIFO] is shown as an example of command-to-command timing for MPC-1. Timing from MPC-1 [WR-FIFO] to MPC-1 [RD-FIFO] is specified in the command-to-command timing table.
3. Seamless MPC-1 [RD-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC-1 [RD-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC-1 [RD-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC-1 [WR-FIFO] commands were executed, then the MPC-1 [RD-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

Figure 39: FIFO READ Operation – ^{t}RPRE = Toggling, ^{t}RPST = 1.5nCK



Notes:
1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. MPC-1 [RD-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC-1. Timing from MPC-1 [RD-FIFO] command to read is ^{t}RTRRD .
3. Seamless MPC-1 [RD-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC-1 [RD-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC-1 [RD-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC-1 [WR-FIFO] commands are executed, then the MPC-1 [RD-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

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Table 89: Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Notes
WR/MWR	MPC-1 [WR FIFO]	^{t}WRWTR	1
	MPC-1 [RD FIFO]	Not allowed	2
	MPC-1 [RD DQ CALIBRATION]	WL + 1+ BL/2+	–
		RU(^{t}WTR /^{t}CK)	
RD	MPC-1 [WR FIFO]	^{t}RTW	4
	MPC-1 [RD FIFO]	Not allowed	2
	MPC-1 [RD DQ CALIBRATION]	^{t}RTRRD	3

Table 89: Timing Constraints for Training Commands (Continued)

Previous Command	Next Command	Minimum Delay	Notes
MPC-1 [WR FIFO]	WR	Not allowed	2
	MPC-1 [WR FIFO]	^{t}CCD	–
	RD	Not allowed	2
	MPC-1 [RD FIFO]	WL + 1 + BL/2+	–
		RU(^{t}WTR /^{t}CK)	
	MPC-1 [RD DQ CALIBRATION]	Not allowed	2
MPC-1 [RD FIFO]	WR	^{t}RTW	4
	MPC-1 [WR FIFO]	^{t}RTW	4
	RD	^{t}RTRRD	3
	MPC-1 [RD FIFO]	^{t}CCD	–
	MPC-1 [RD DQ CALIBRATION]	^{t}RTRRD	3
MPC-1 [RD DQ CALIBRATION]	WR	^{t}RTW	4
	MPC-1 [WR FIFO]	^{t}RTW	4
	RD	^{t}RTRRD	3
	MPC-1 [RD FIFO]	Not allowed	2
	MPC-1 [RD DQ CALIBRATION]	^{t}CCD	–

Notes:
1. ^{t}WRWTR = (WL + BL/2)/^{t}CK + RU(^{t}DQSS (MAX)) + MAX(7.5ns, 8nCK).
2. No commands are allowed between MPC-1 [WR FIFO] and MPC-1 [RD FIFO] except the MRW commands related to training parameters.
3. ^{t}RTRRD = (RL + BL/2)/^{t}CK + ^{t}DQSCK (MAX) + MAX(7.5ns, 8nCK) + ^{t}RPST.
4. ^{t}RTW = RL + BL/2 + RU(^{t}DQSCK (MAX)) + (ODT $_{ON(MAX)}$ - ODT $_{ON(MIN)}$)) - WL + ^{t}WPRE + ^{t}WPST.

ZQ Calibration

The MPC command is used to initiate ZQ calibration, which calibrates the output driver impedance and CA/DQ ODT impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation and is designed to eliminate any need for coordination between channels (i.e., it allows for channel independence). ZQ calibration is required each time that the PU-Cal value (MR3-OP[0]) is changed. Additional ZQ calibration commands may be required as the voltage and temperature change in the system environment. CA ODT values (MR11-OP[6:4]) and DQ ODT values (MR11-OP[2:0]) may be changed without performing ZQ calibration, as long as the PU-Cal value doesn't change.

There are two ZQ calibration modes initiated with the MPC command: ZQCALSTART and ZQCALLATCH. ZQCALSTART initiates the calibration procedure, and ZQCalLatch captures the result and loads it into the drivers.

A ZQCALSTART command may be issued anytime the device is not in a power-down state. A ZQCALLATCH command may be issued anytime outside of power-down after ^{t}ZQCAL has expired and all DQ bus operations have completed. The CA bus must maintain a deselect state during ^{t}ZQLAT to allow CA ODT calibration settings to be updated. The DQ calibration value will not be updated until ZQCALLATCH is performed and

^{t}ZQLAT has been met. The following mode register fields that modify I/O parameters cannot be changed following a ZQCALSTART command and before ^{t}ZQCAL has expired:

- PU-Cal (pull-up calibration V_{OH} point)
- PDDS (pull-down drive strength and Rx termination)
- DQ-ODT (DQ ODT value)
- CA-ODT (CA ODT value)

ZQCALRESET Command

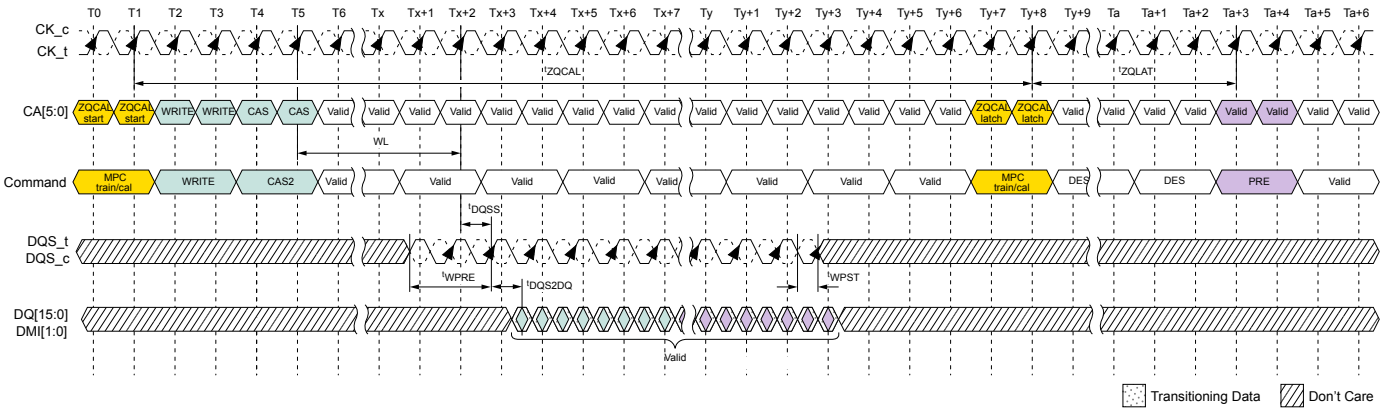
The ZQCALRESET command resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCALSTART and ZQCALLATCH commands are not used.

The ZQCALRESET command is executed by writing MR10-OP[0] = 1_B.

Table 90: ZQ Calibration Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ calibration time	^{t}ZQCAL	MAX	1	us
ZQ calibration latch time	^{t}ZQLAT	MAX	MAX(30ns, 8nCK)	ns
ZQ calibration reset time	^{t}ZQRESET	MAX	MAX(50ns, 3nCK)	ns

Figure 40: ZQCal Timing



Notes:
1. WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the ^{t}ZQCAL time and prior to latching the results.
2. Before the ZQCALLATCH command can be executed, any prior commands that utilize the DQ bus must have completed. WRITE commands with DQ termination must be given enough time to turn off the DQ ODT before issuing the ZQCALLATCH command. See the ODT section for ODT timing.

Multichannel Considerations

The device includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

- The ZQCALSTART command can be issued to either or both channels.
- The ZQCALSTART command can be issued when either or both channels are executing other commands, and other commands can be issued during ^{t}ZQCAL.
- The ZQCALSTART command can be issued to both channels simultaneously.
- The ZQCALSTART command will begin the calibration unless a previously requested ZQ calibration is in progress.
- If the ZQCALSTART command is received while a ZQ calibration is in progress, the command will be ignored and the in-progress calibration will not be interrupted.
- The ZQCALLATCH command is required for each channel.
- The ZQCALLATCH command can be issued to both channels simultaneously.
- The ZQCALLATCH command will latch results of the most recent ZQCALSTART command provided ^{t}ZQCAL has been met.
- ZQCALLATCH commands that do not meet ^{t}ZQCAL will latch the results of the most recently completed ZQ calibration.
- The ZQRESET MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCALSTART and ZQCALLATCH commands as needed without regard to the state of the other channel.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm, ±1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel must use a separate ZQCAL resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCAL's don't overlap

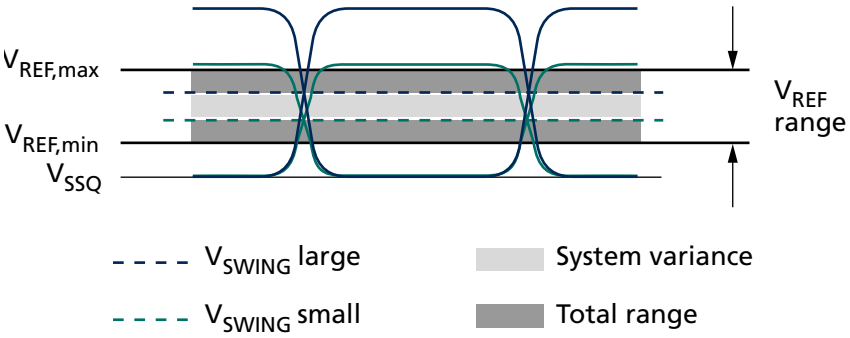
The total capacitive loading on the ZQ pin must be limited to 5pF. For example, if a system configuration shares a CA bus between *n* channels to form an n ×16 wide bus, and no means are available to control the ZQCAL separately for each channel (i.e. separate CS, CKE, or CK), then each x16 channel must have a separate ZQCAL resistor. For a x32, two-rank system, each x16 channel must have its own ZQCAL resistor, but the ZQCAL resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCAL commands for Rank[0] and Rank[1] don't overlap.

$V_{REF(DQ)}$ Training

The device's internal $V_{REF(DQ)}$ specification parameters are operating voltage range, step size, V_{REF} step time, V_{REF} full-range step time, and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 devices. The minimum range is defined by $V_{REF,max}$ and $V_{REF,min}$.

Figure 41: V_{REF} Operating Range ($V_{REF,max}$, $V_{REF,min}$)

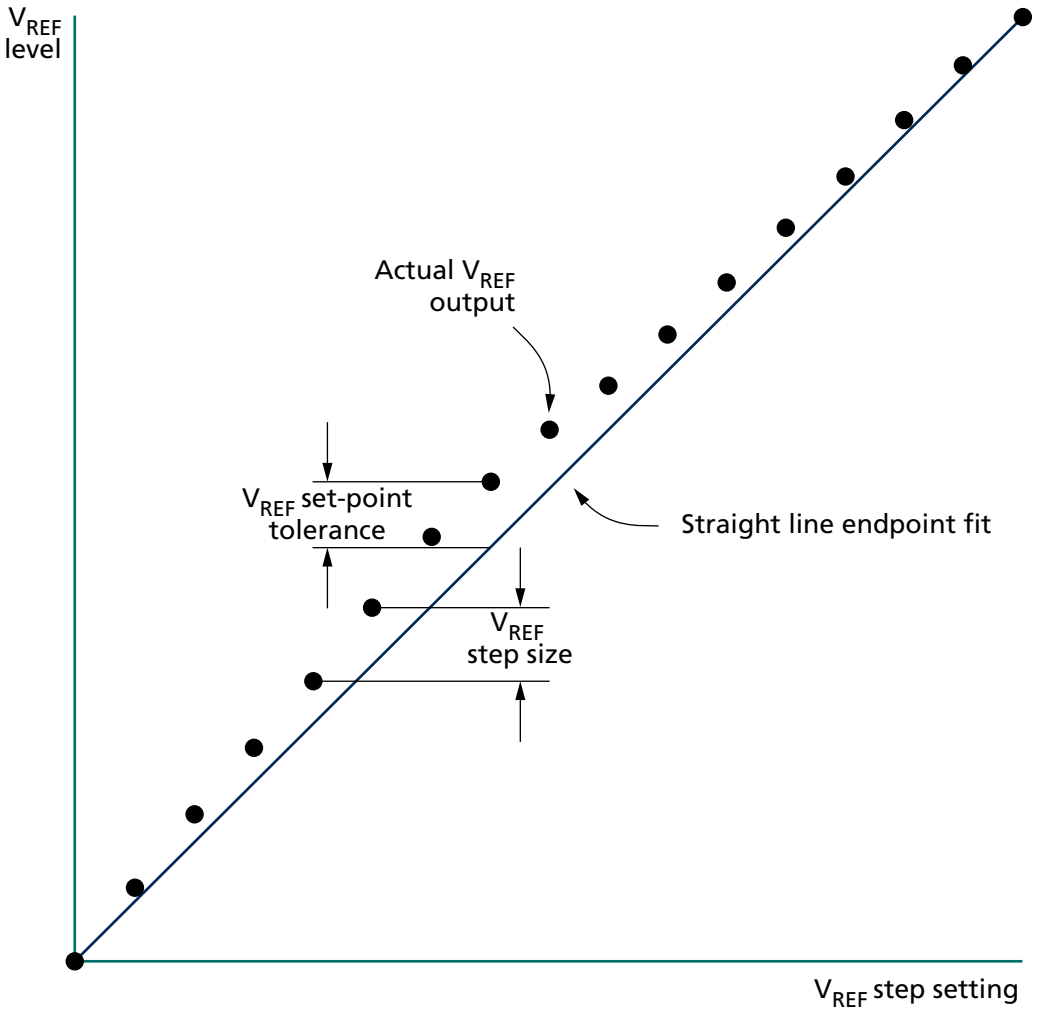


The V_{REF} step size is defined as the step size between adjacent steps. V_{REF} step size ranges from 0.3% × V_{DDQ} to 0.5% × V_{DDQ}. However, for a given design, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of the number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the two endpoints, where the endpoints are at the minimum and maximum V_{REF} values for a specified range.

Figure 42: V_{REF} Set-Point Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by ^{t}VREF_SHORT and ^{t}VREF_LONG. The parameters are defined from t0 to t1, where t1 is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance (V_{REF,val_tol}).

The V_{REF} valid level is defined by V_{REF,val_tol} to qualify the step time t1 (see the following figures). This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for LPDDR4 component level validation/characterization.

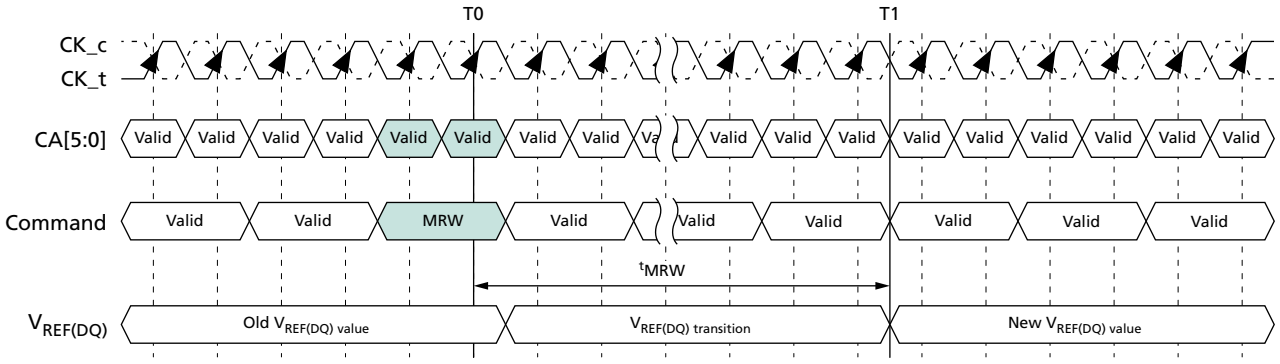
^{t}VREF_SHORT is for a single step size increment/decrement change in the V_{REF} voltage.

^{t}VREF_LONG is the time including up to the full range of V_{REF} (MIN to MAX or MAX to MIN).

t0 is referenced to MRW command clock.

t1 is referenced to V_{REF,val_tol}.

Figure 43: $V_{REF(DQ)}$ Transition Time for Short or Long Changes



A MRW command to MR14-OP[5:0] will set the $V_{REF(DQ)}$ value. The minimum time required between two V_{REF} MRW commands is ^{t}VREF_SHORT for a single step and ^{t}VREF_LONG for (up to) a full voltage range step.

Figure 44: $V_{REF(DQ)}$ Single-Step Increment

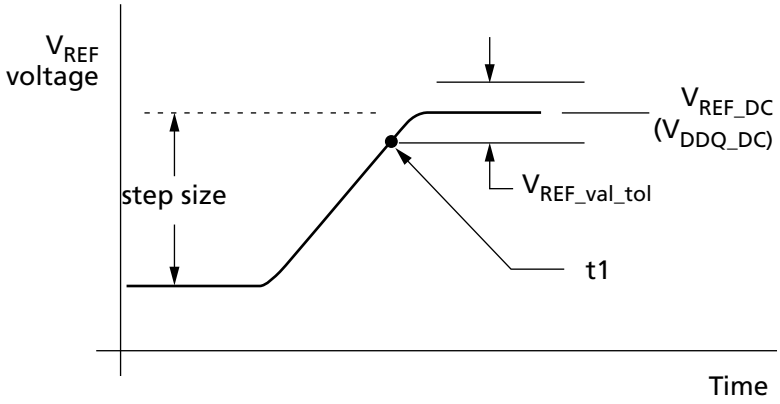


Figure 45: $V_{REF(DQ)}$ Single-Step Decrement

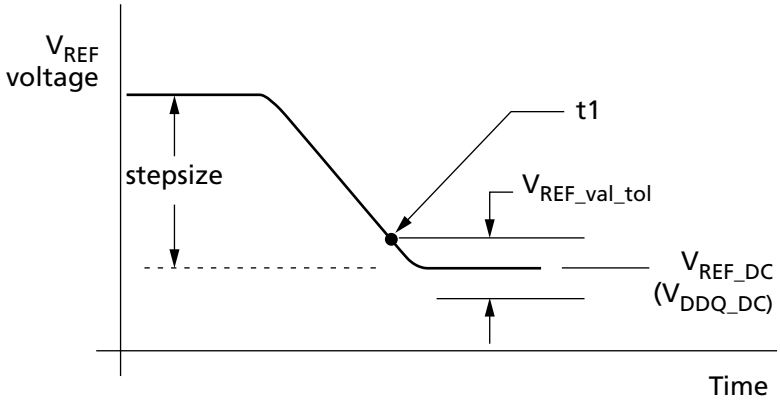


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Figure 46: $V_{REF(DQ)}$ Full Step from $V_{REF,min}$ to $V_{REF,max}$

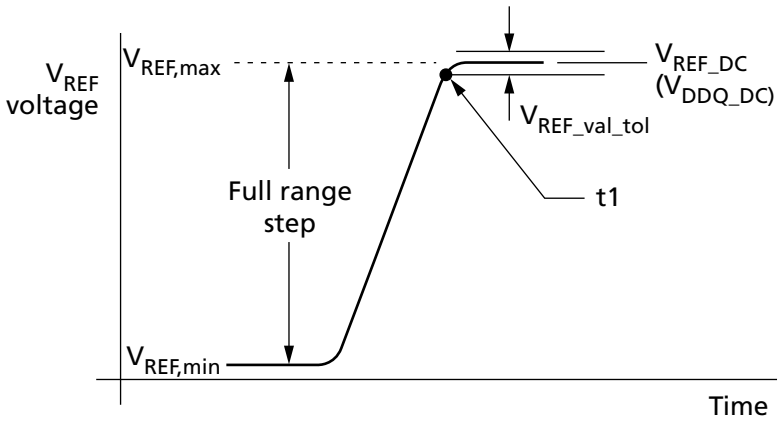
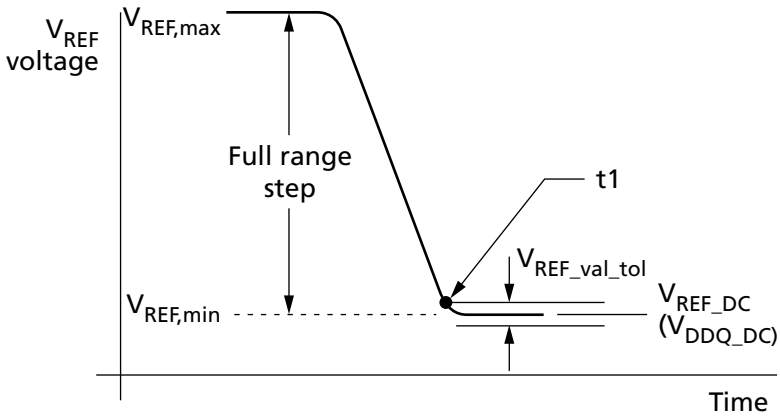


Figure 47: $V_{REF(DQ)}$ Full Step from $V_{REF,max}$ to $V_{REF,min}$



The following table contains the DQ internal V_{REF} specification that will be characterized at the component level for compliance. The component level characterization method is TBD.

Table 91: Internal $V_{REF(DQ)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(DQ),max\_r1}$	$V_{REF(DQ)}$ range-0 MAX operating point	42%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r1}$	$V_{REF(DQ)}$ range-0 MIN operating point	–	–	22%	V_{DDQ}	1, 11
$V_{REF(DQ),max\_r2}$	$V_{REF(DQ)}$ range-1 MAX operating point	30%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r2}$	$V_{REF(DQ)}$ range-1 MIN operating point	–	–	10%	V_{DDQ}	1, 11
$V_{REF(DQ),step}$	$V_{REF(DQ)}$ step size	0.30%	0.40%	0.50%	V_{DDQ}	2
$V_{REF(DQ),set\_tol}$	$V_{REF(DQ)}$ set tolerance	–1.00%	0.00%	1.00%	V_{DDQ}	3, 4, 6
		–0.10%	0.00%	0.10%	V_{DDQ}	3, 5, 7

Table 91: Internal $V_{REF(DQ)}$ Specifications (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
^{t}VREF_SHORT	$V_{REF(DQ)}$ step time	–	–	80	ns	8
^{t}VREF_LONG		–	–	200	ns	9
$V_{REF(DQ),val\_tol}$	$V_{REF(DQ)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

Notes:
1. $V_{REF(DQ)}$ DC voltage referenced to V_{DDQ_DC}.
2. $V_{REF(DQ)}$ step size increment/decrement range. $V_{REF(DQ)}$ at DC level.
3. $V_{REF(DQ),new} = V_{REF(DQ),old} \pm n \times V_{REF(DQ),step}$; n = number of steps; if increment, use "+"; if decrement, use "-".
4. The minimum value of $V_{REF(DQ)}$setting tolerance = $V_{REF(DQ),new}$ - 1.0% × V_{DDQ}. The maximum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 1.0% × V_{DDQ}. For n >4.
5. The minimum value of $V_{REF(DQ)}$setting tolerance = $V_{REF(DQ),new}$ - 1.0% × V_{DDQ}. The maximum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 1.0% × V_{DDQ}. For n <4.
6. Measured by recording the MIN and MAX values of the $V_{REF(DQ)}$ output over the range, drawing a straight line between those points and comparing all other $V_{REF(DQ)}$ output settings to that line.
7. Measured by recording the MIN and MAX values of the $V_{REF(DQ)}$ output across 4 consecutive steps (n = 4), drawing a straight line between those points and comparing all other $V_{REF(DQ)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(DQ)}$.
9. Time from MRW command to increment or decrement more than one step size up to a full range of $V_{REF(DQ)}$.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR14-OP[6].

Write Leveling

To improve signal-integrity performance, the device provides a write-leveling feature to compensate for CK-to-DQS timing skew, affecting timing parameters such as ^{t}DQSS, ^{t}DSS, and ^{t}DSH. The memory controller uses the write-leveling feature to receive feedback from the device, enabling it to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair. The memory controller performing the training must have an adjustable delay setting on the DQS_t/DQS_c signal pair to align the rising edge of DQS signals with that of the clock signal at the device pin. The device asynchronously feeds back CK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signal delay established through this exercise ensures the ^{t}DQSS specification can be met.

All data bits (DQ[7:0] for DQS[0], and DQ[15:8] for DQS[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels.

The device enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the WRITE LEVELING operation. Upon completion of the WRITE LEVELING operation, the device exits from write-leveling mode when MR2-OP[7] is reset LOW.

Write leveling should be performed before write training (DQS2DQ training).

Write Leveling Procedure

The controller drives DQS_t LOW and DQS_c HIGH after a delay of ^{t}WLDQSEN. After time ^{t}WLMRD , the controller provides at least 2 pulses of DQS signal input, which is used by the device to sample the clock signal driven from the controller. The delay time ^{t} WLMRDMAX is controller-dependent. The device guarantees a valid output starting from the second edge and every edge thereafter, and provides asynchronous feedback on all the DQ bits after time ^{t}WLO. The controller samples this information and either increments or decrements the DQS_t and/or DQS_c delay settings and launches the next DQS_t/DQS_c pulse.

The sample time and trigger time are controller-dependent. After the following DQS_t/DQS_c transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device.

Figure 48: Write Leveling Timing – ^{t}DQSL (MAX)

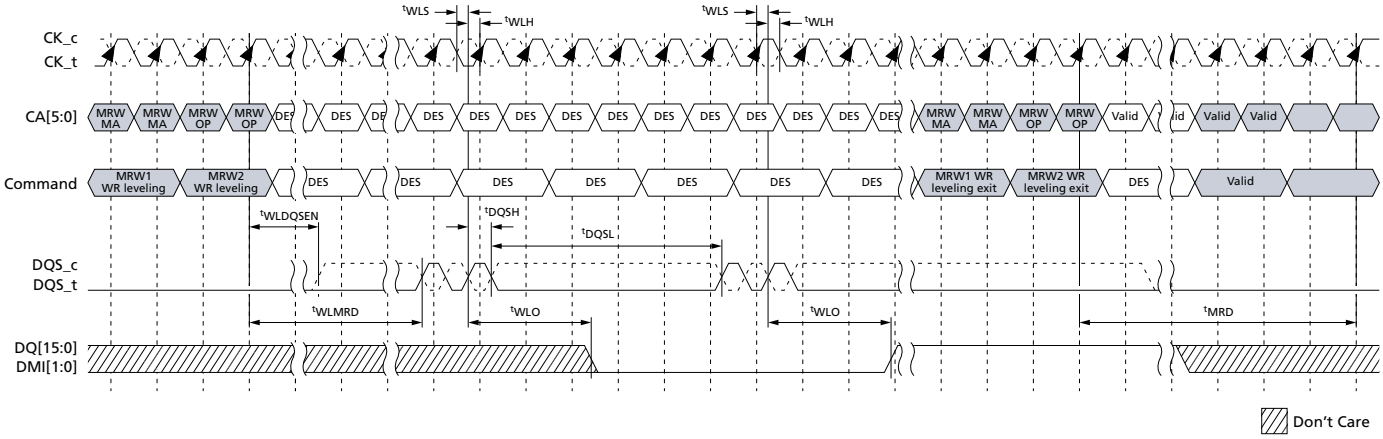

tWLS
tWLH
tWLS
tWLH
CK_c
CK_t
CA[5:0]
MRW MA
MRW OP
DES
Valid
Command
MRW1 WR leveling
MRW2 WR leveling
MRW1 WR leveling exit
MRW2 WR leveling exit
tWLDQSEN
tDQSH
tDQSL
DQS_c
DQS_t
tWLMRD
tWLO
tWLO
tMRD
DQ[15:0]
DMI[1:0]
Don't Care

Figure 49: Write Leveling Timing – ^{t}DQSL (MIN)

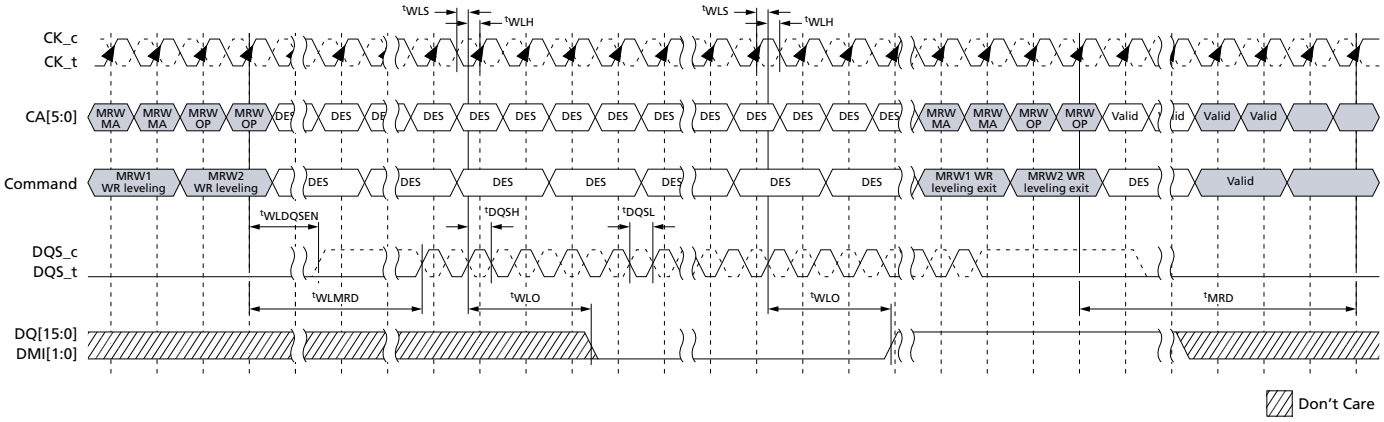


Table 92: Write-Leveling Timing Parameters

Parameter	Symbol	Min/Max	Speed Grade								Units
			533	1066	1600	2133	2667	3200	3733	4267	
DQS_t/DQS_c delay after write leveling mode is programmed	^{t}WLDQSEN	Min									^{t}CK
		Max	20								
First DQS_t/DQS_c edge after write leveling mode is programmed	^{t}WLMRD	Min	40								^{t}CK
		Max	–								
Write leveling output delay	^{t}WLO	Min	0								ns
		Max	20								
Write leveling setup time	^{t}WLS	Min	135				TBD	TBD	TBD	TBD	ps
Write leveling hold time	^{t}WLH	Max	135				TBD	TBD	TBD	TBD	ps
Mode register set command delay	^{t}MRD	Min	MAX (14ns, 10nCK)								ns
		Max	–								

Proposal

Write Training

The device uses an unmatched DQS-DQ path to enable high-speed performance and save power. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye. The DQ receiver is located at the DQ pad and has a shorter internal delay than the DQS signal. The DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and write training is accomplished by delaying the DQ signals relative to DQS such that the data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available:

- Command-based FIFO WR/RD with user patterns
- An internal DQS clock-tree oscillator, which determines the need for, and the magnitude of, required training

The command-based FIFO WR/RD uses the MPC-1 command with operands to enable this special mode of operation. When issuing the MPC-1 command, if CA[5] is set LOW (OP[6] = 0), then the device will perform a NOP command. When CA[5] is set HIGH, the CA[4:0] pins enable training functions or are reserved for future use (RFU). MPC-1 commands that initiate a read or write to the device must be followed immediately by a CAS-2 command. See the MPC Operation section for more information.

To perform write training, the controller can issue an MPC-1 [WRITE DQ FIFO] command with OP[6:0] set, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a WRITE DQ FIFO. Timings for MPC-1 [WRITE DQ FIFO] are identical to WRITE commands, with WL timed from the second rising clock edge of the CAS-2 command. Up to five consecutive MPC-1 [WRITE DQ FIFO] commands with user-defined patterns may be issued to the device, which will store up to 80 values (BL16 × 5) per pin that can be read back via the MPC-1 [READ DQ FIFO] command. (The WRITE/READ FIFO POINTER operation is described in a different section.

After writing data with the MPC-1 [WRITE DQ FIFO] command, the data can be read back with the MPC-1 [READ DQ FIFO] command and results can be compared with "expected" data to determine whether further training (DQ delay) is needed. MPC-1 [READ DQ FIFO] is initiated by issuing an MPC-1 command, as described in in the MPC Operation section, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC-1 [READ DQ FIFO] command are identical to READ commands, with RL timed from the second rising clock edge of the CAS-2 command.

READ DQ FIFO is nondestructive to the data captured in the FIFO; data may be read continuously until it is disturbed by another command, such as a READ, WRITE, or another MPC-1 [WRITE DQ FIFO]. If fewer than five WRITE DQ FIFO commands are executed, unwritten registers will have undefined (but valid) data when read back.

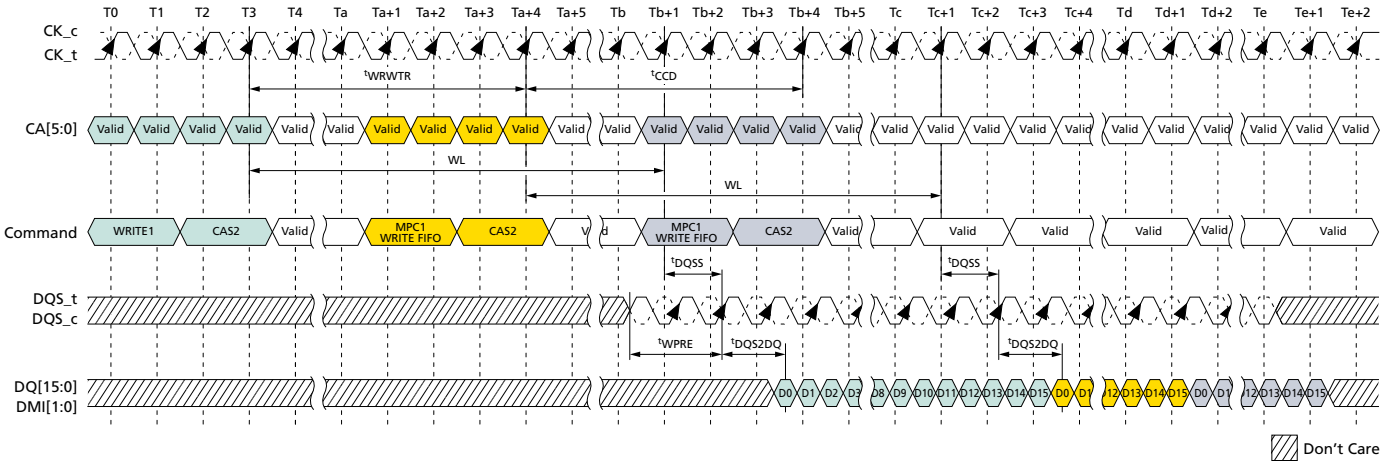
For example: If five WRITE DQ FIFO commands are executed sequentially, then a series of READ DQ FIFO commands will read valid data from FIFO[0], FIFO[1]….FIFO[4] and then wrap back to FIFO[0] on the next READ DQ FIFO. However, if fewer than five WRITE DQ FIFO commands are executed sequentially (example = 3), then a series of READ DQ FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two READ DQ FIFO commands will return undefined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

The write DQ FIFO pointer is reset under the following conditions:

- Power-up initialization
- RESET_n asserted
- Power-down entry
- Self refresh power-down entry

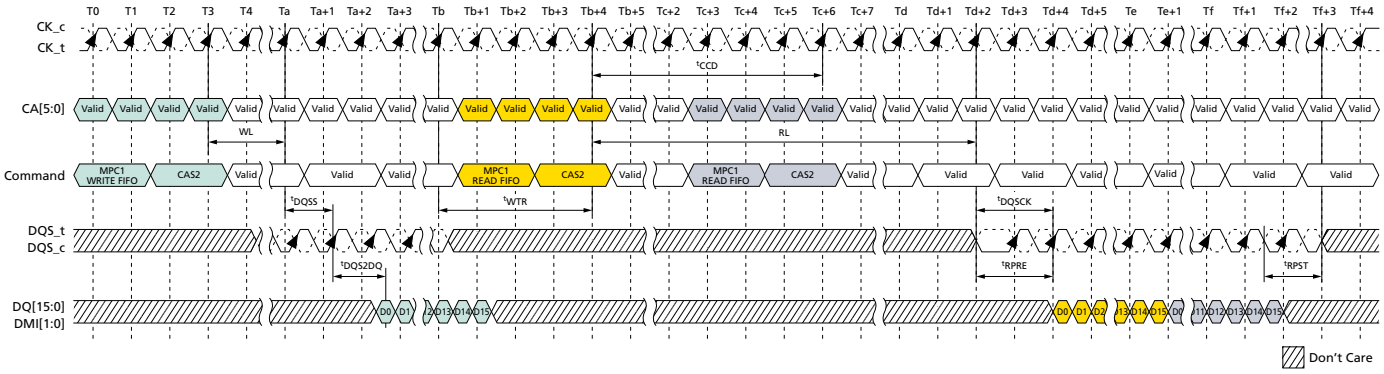
The WR-FIFO and RD-FIFO pointers both advance for any normal (non-FIFO) READ operation (RD, RDA). An MPC-1 [WRITE DQ FIFO] command advances the WR-FIFO pointer, and an MPC-1 [READ DQ FIFO] command advances the RD-FIFO pointer. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction:

Figure 50: MPC-1 (WR-FIFO) Operation – ^{t}WPRE = 2nCK, ^{t}WPST = 0.5nCK



Notes:
1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh, with CKE HIGH.
2. Write-1 to MPC-1 is shown as an example of command-to-command timing for MPC-1. Timing from write-1 to MPC-1 [WR-FIFO] is ^{t}WRWTR.
3. Seamless MPC-1 [WR-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC-1 [WR-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS, ^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of 5 MPC-1 [WR-FIFO] commands may be executed consecutively without corrupting FIFO data. The 6th MPC-1 [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC-1 [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other commands in between. See Write Training for more information on FIFO pointer behavior.

Figure 51: MPC-1 [RD-FIFO] Operation – ^{t}WPRE = 2nCK, ^{t}WPST = 0.5nCK, ^{t}RPRE = Toggling, ^{t}RPST = 1.5nCK



Notes:

1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. MPC-1 [WR-FIFO] to MPC-1 [RD-FIFO] is shown as an example of command-to-command timing for MPC-1. Timing from MPC-1 [WR-FIFO] to MPC-1 [RD-FIFO] is specified in the command-to-command timing table.
3. Seamless MPC-1 [RD-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC-1 [RD-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC-1 [RD-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC-1 [WR-FIFO] commands were executed, then the MPC-1 [RD-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

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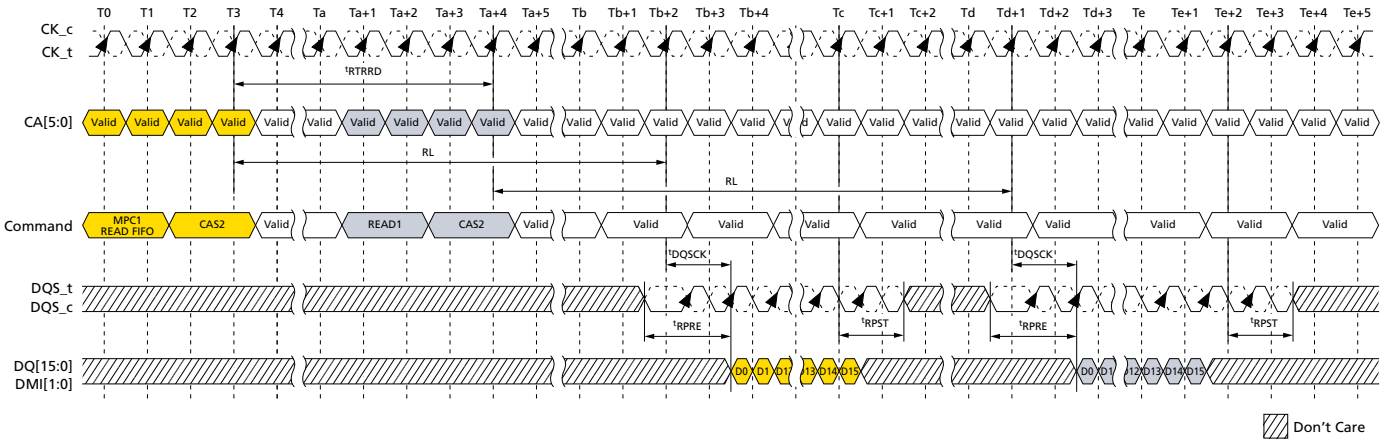
Figure 52: FIFO READ-to-READ Operation – tRPRE = Toggling, tRPST = 1.5nCK



Notes:
1. MPC-1 [WR-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. MPC-1 [RD-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC-1. Timing from MPC-1 [RD-FIFO] command to read is tRTRRD .
3. Seamless MPC-1 [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC-1 [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC-1 [RD-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC-1 [WR-FIFO] commands are executed, then the MPC-1 [RD-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC-1 command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

Internal Interval Timer

As voltage and temperature change on the device, the DQS clock-tree delay will shift, requiring retraining. The device includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS oscillator will provide the controller with important information regarding the need to retrain and the magnitude of potential error.

The DQS interval oscillator is started by issuing an MPC command with OP[5:0] = 001011b, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS oscillator may be stopped by issuing an MPC-1 [STOP DQS OSC] command with OP[6:0] set, as described in MPC Operation, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS oscillator, then the MPC-1 [STOP DQS OSC] command should not be used (illegal). When the DQS oscilla-

tor is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS interval oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation, where run time = total time between start and stop commands and DQS delay = the value of the DQS clock tree delay (^{t}DQS2DQ MIN/MAX):

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{run time}}$$

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific. Therefore, the total accuracy of the DQS oscillator counter is given by:

$$\text{DQS oscillator accuracy} = 1 - \text{granularity error} - \text{matching error}$$

For example, if the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 800ps (^{t}DQS2DQ MAX), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{100\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 12.8ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

For example, running the DQS oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum DQS clock tree delay is 800ps (^{t}DQS2DQ MAX), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{500\text{ns}} = 0.32\%$$

This equates to a granularity timing error or 2.56ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delays that can be counted within the run time, determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0].

MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received.

The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, the memory controller must assume that the counter overflowed the register and therefore discard the result. The longest run time for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest runtime interval} = 2^{16} \times {}^{t}\text{DQS2DQ(min)} = 2^{16} \times 0.2\text{ns} = 13.1\text{us}$$

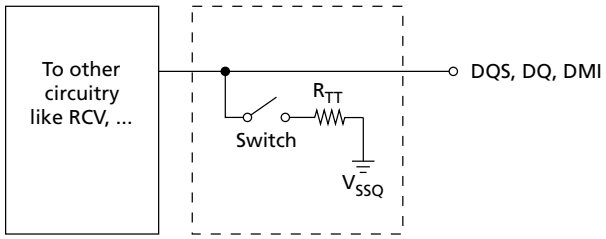
DQ On-Die-Termination

On-die termination (ODT) is a feature that enables the device to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during WRITE or MASK WRITE operation.

The ODT feature is off and cannot be supported in power-down and self refresh modes.

A simple functional representation of the ODT feature is shown below.

Figure 53: Functional Representation of On-Die-Termination



The switch is enabled by the internal ODT control logic, which uses the WRITE-1 or MASK WRITE-1 command and other mode register control information. The value of R_{TT} is determined by the settings of mode register bits.

ODT Mode Register

The ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of R_{TT} is determined by the settings of those bits. The ODT mode is disabled if MR11 OP[2:0] = 0.

Asynchronous ODT

When ODT mode is enabled in MR11 OP[2:0], DRAM ODT is always High-Z. The DRAM ODT feature is automatically turned ON asynchronously after a WRITE-1, MASK WRITE-1, or MPC (FIFO WRITE) command. After the burst write is complete, the DRAM ODT turns OFF asynchronously. The DQ bus ODT control is automatic and will turn the ODT resistance on/off if DQ-ODT is enabled in the mode register.

The following timing parameters apply when the DQ bus ODT is enabled:

- ODTLon, ^{t}ODTon,min, ^{t}ODTon,max
- ODTLoff, ^{t}ODToff,min, ^{t}ODToff,max

$ODTL_{ON}$ is a synchronous parameter and is the latency from a WRITE-1, MASK WRITE-1, or MPC (FIFO WRITE) command to the ^{t}ODTon reference. $ODTL_{ON}$ latency is a fixed latency value for each speed bin. Each speed bin has a different $ODTL_{ON}$ latency.

Minimum R_{TT} turn-on time (^{t}ODTon,min) is the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on.

Maximum R_{TT} turn on time (^{t}ODTon,max) is the point in time when the ODT resistance is fully on.

^{t}ODTon,min and ^{t}ODTon,max are measured once $ODTL_{on}$ latency is satisfied from CAS-2 command.

$ODTL_{OFF}$ is a synchronous parameter and it is the latency from CAS-2 command to ^{t}ODToff reference. $ODTL_{OFF}$ latency is a fixed latency value for each speed bin. Each speed bin has a different $ODTL_{OFF}$ latency.

Minimum R_{TT} turn-off time (^{t}ODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (^{t}ODToff,max) is the point in time when the on-die termination has reached High-Z.

^{t}ODToff,min and ^{t}ODToff,max are measured once $ODTL_{off}$ latency is satisfied from CAS-2 command.

Table 93: $ODTL_{ON}$ and $ODTL_{OFF}$ Latency Values

$ODTL_{ON}$ Latency[1]				$ODTL_{OFF}$ Latency[2]		Lower Frequency Limit (>) (MHz)	Upper Frequency Limit (≤) (MHz)
^{t}WPRE = 1 ^{t}CK		^{t}WPRE = 2 ^{t}CK					
WL Set A (nCK)	WL Set B (nCK)	WL Set A (nCK)	WL Set B (nCK)	WL Set A (nCK)	WL Set B (nCK)		
N/A	N/A	N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	N/A	N/A	266	533
4	8	N/A	6	18	22	533	800
4	12	4	12	20	28	800	1066
6	16	4	14	22	32	1066	1333
6	18	6	18	24	36	1333	1600
8	22	6	20	26	40	1600	1866
8	24	8	24	28	44	1866	2133

Notes: 1. $ODTL_{ON}$ is referenced from CAS-2 command.
2. $ODTL_{OFF}$ as shown in table assumes BL = 16. For BL32, 8 ^{t}CK should be added.

Table 94: Asynchronous ODT Turn On and Turn Off Timing

Parameter	800–2133 MHz	Unit
^{t}ODTon,min	1.5	ns
^{t}ODTon,max	3.5	ns
^{t}ODToff,min	1.5	ns
^{t}ODToff,max	3.5	ns

Figure 54: Asynchronous ODT_{ON} Timing – $^{t}WPRE$ = 1*n*CK, $^{t}DQSS$ = Nominal

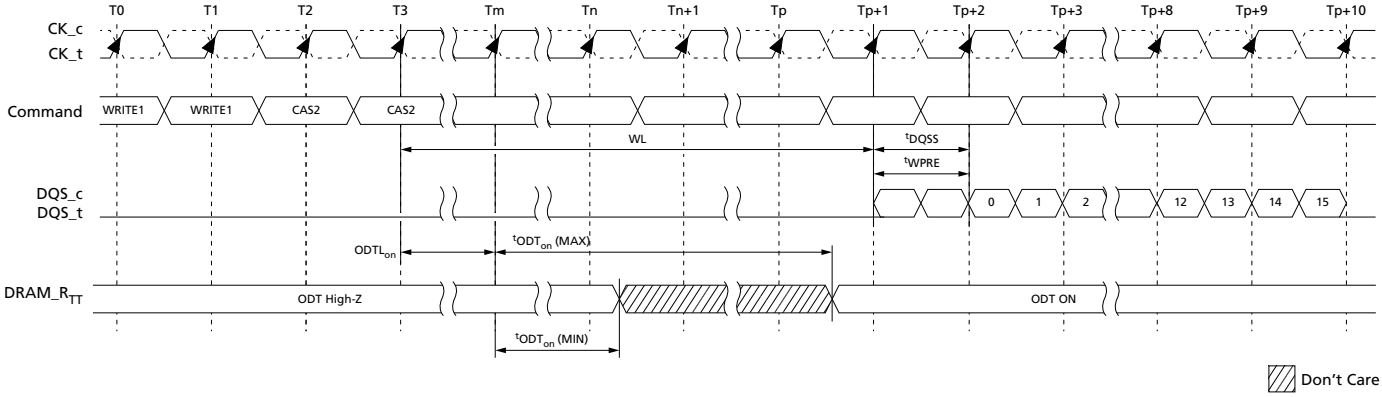


Figure 55: Asynchronous ODT_{ON} Timing – $^{t}WPRE$ = 2*n*CK, $^{t}DQSS$ = Nominal

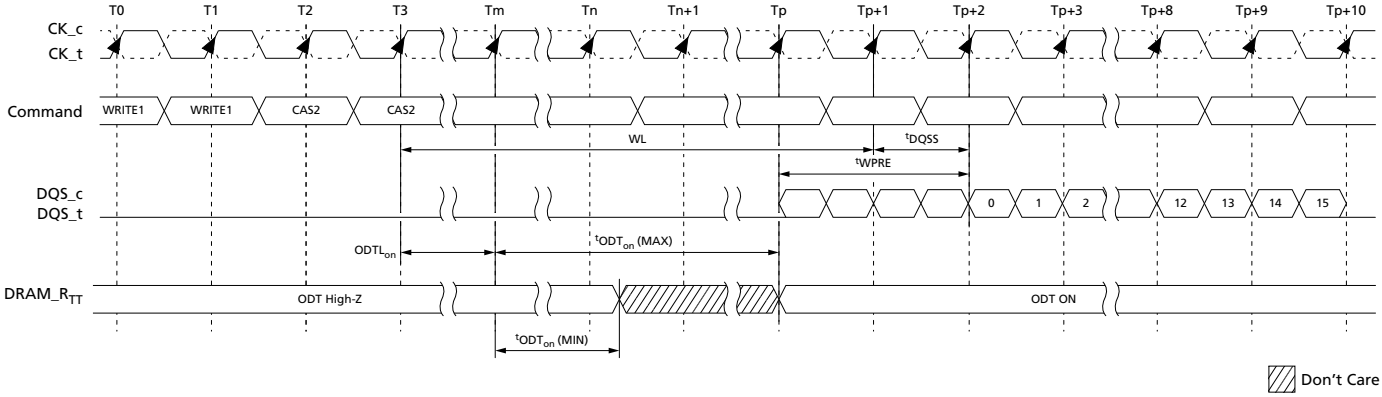


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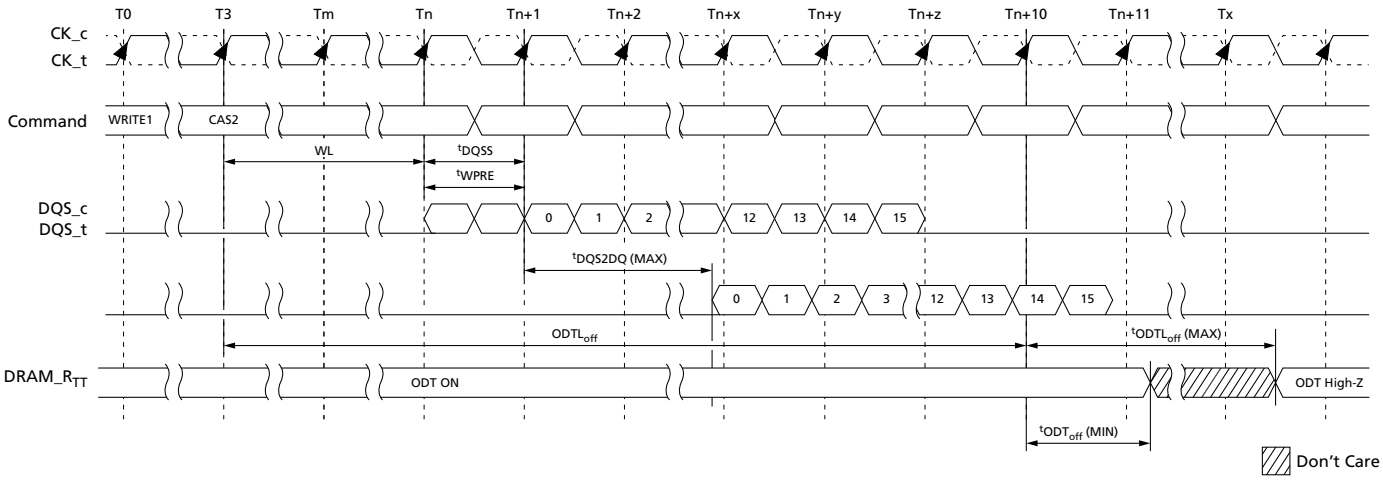
Figure 56: Asynchronous ODT_{OFF} Timing – $^{t}WPRE$ = 1*n*CK, $^{t}DQSS$ = Nominal



DQ ODT During Power-Down and Self Refresh Modes

DQ bus ODT will be disabled in power-down mode. In self refresh mode, the ODT will be turned off when CKE is LOW but will be enabled if CKE is HIGH and DQ ODT is enabled in the mode register.

ODT During Write-Leveling Mode

If ODT is enabled in MR11 OP[2:0] in write-leveling mode, the device always provides the termination on DQS_t/DQS_c signals. DQ termination is always off in the write-leveling mode.

Table 95: Termination State in Write-Leveling Mode

ODT State in MR11 OP[2:0]	DQS Termination	DQ[15:0]/DMI[1:0] Termination
Disabled	Off	Off
Enabled	On	Off

Data Mask and Data Bus Inversion (DBI[DC]) Function

Data mask (DM) is supported for WRITE operations and the data bus inversion DBI(DC) is supported for READ, WRITE, MASK WRITE, MRR, and MRW operations. DM and DBI(DC) functions are supported with byte granularity. DBI(DC) for READ operations (READ, MRR) can be enabled or disabled via MR3 OP[6]. DBI(DC) for WRITE operations (WRITE, MASK WRITE, MRW) can be enabled or disabled via MR3 OP[7]. DM for MASK WRITE operations can be enabled or disabled via MR13 OP[5]. The device has one data mask inversion (DMI) pin per byte and a total of two DMI pins per channel. The DMI signal is a bidirectional DDR signal, is sampled with the DQ signals, and is electrically identical to a DQ signal.

There are eight possible states for the device with the DM and DBI(DC) functions.

Table 96: Function Behavior of DMI Signal During WRITE, MASKED WRITE, and READ Operations

DM Function	Write DBI(DC)	Read DBI(DC)	DMI Signal During WRITE Command	DMI Signal During MASKED WRITE Command	DMI Signal During READ Command	DMI Signal During MPC WR FIFO	DMI Signal During MPC RD FIFO	DMI Signal During MPC DQ READ Calibration
Disabled	Disabled	Disabled	"Don't Care"[1]	Illegal[1, 3]	High-Z[2]	"Don't Care"[1]	High-Z[2]	High-Z[2]
Disabled	Enabled	Disabled	DBI(DC)[4]	Illegal[3]	High-Z[2]	Train[9]	Train[10]	Train[11]
Disabled	Disabled	Enabled	"Don't Care"[1]	Illegal[3]	DBI(DC)[5]	Train[9]	Train[10]	Train[11]
Disabled	Enabled	Enabled	DBI(DC)[4]	Illegal[3]	DBI(DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Disabled	"Don't Care"[6]	DM[7]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Disabled	DBI(DC)[4]	DBI(DC)[8]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Enabled	"Don't Care"[6]	DM[7]	DBI(DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Enabled	DBI(DC)[4]	DBI(DC)[8]	DBI(DC)[5]	Train[9]	Train[10]	Train[11]

Notes:
1. The DMI input signal is "Don't Care." DMI input receivers are turned off.
2. DMI output drivers are turned off.
3. The MASK WRITE command is not allowed and is considered an illegal command when the DM function is disabled.
4. The DMI signal is treated as DBI and indicates whether the device needs to invert the write data received on DQs within a byte. The device inverts write data received on the DQ inputs if DMI is sampled HIGH and leaves the write data non-inverted if DMI is sampled LOW.
5. The device inverts read data on its DQ outputs associated within a byte and drives the DMI signal HIGH when more than four data bits =1 within a given byte lane; otherwise, the device does not invert the read data and drives DMI signal LOW.
6. The device does not perform a MASK operation when it receives a WRITE (or MRW) command. During the WRITE burst, the DMI signal is "Don't Care" and is ignored.
7. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The DMI signal is treated as a data mask (DM) and indicates which bytes within a burst will be masked. When the DMI signal is sampled HIGH, the device masks that beat of the burst for the given byte lane. All DQ input signals within a byte are "Don't Care"

(either HIGH or LOW) when DMI is HIGH. When the DMI signal is sampled LOW, the device does not perform a MASK operation and data received on the DQ inputs is written to the array.

8. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The device masks the write data received on the DQ inputs if five or more data bits =1 on DQ[2:7] or DQ[10:15] (for lower byte or upper byte respectively) and the DMI signal is LOW. Otherwise, the device does not perform the MASK operation and treats it as a legal DBI pattern. The DMI signal is treated as a DBI signal, and data received on the DQ input is written to the array.
9. The DMI signal is treated as a training pattern. The device does not perform any MASK operation and does not invert write data received on the DQ inputs.
10. The DMI signal is treated as a training pattern. The device returns the data pattern written to the WR FIFO.
11. The DMI signal is treated as a training pattern. For more information, see the MPC DQ Read Training section.

Figure 57: MASK WRITE Command With DM and DBI Enabled: ^{t}WPRE = 2nCK and ^{t}WPST = 0.5nCK

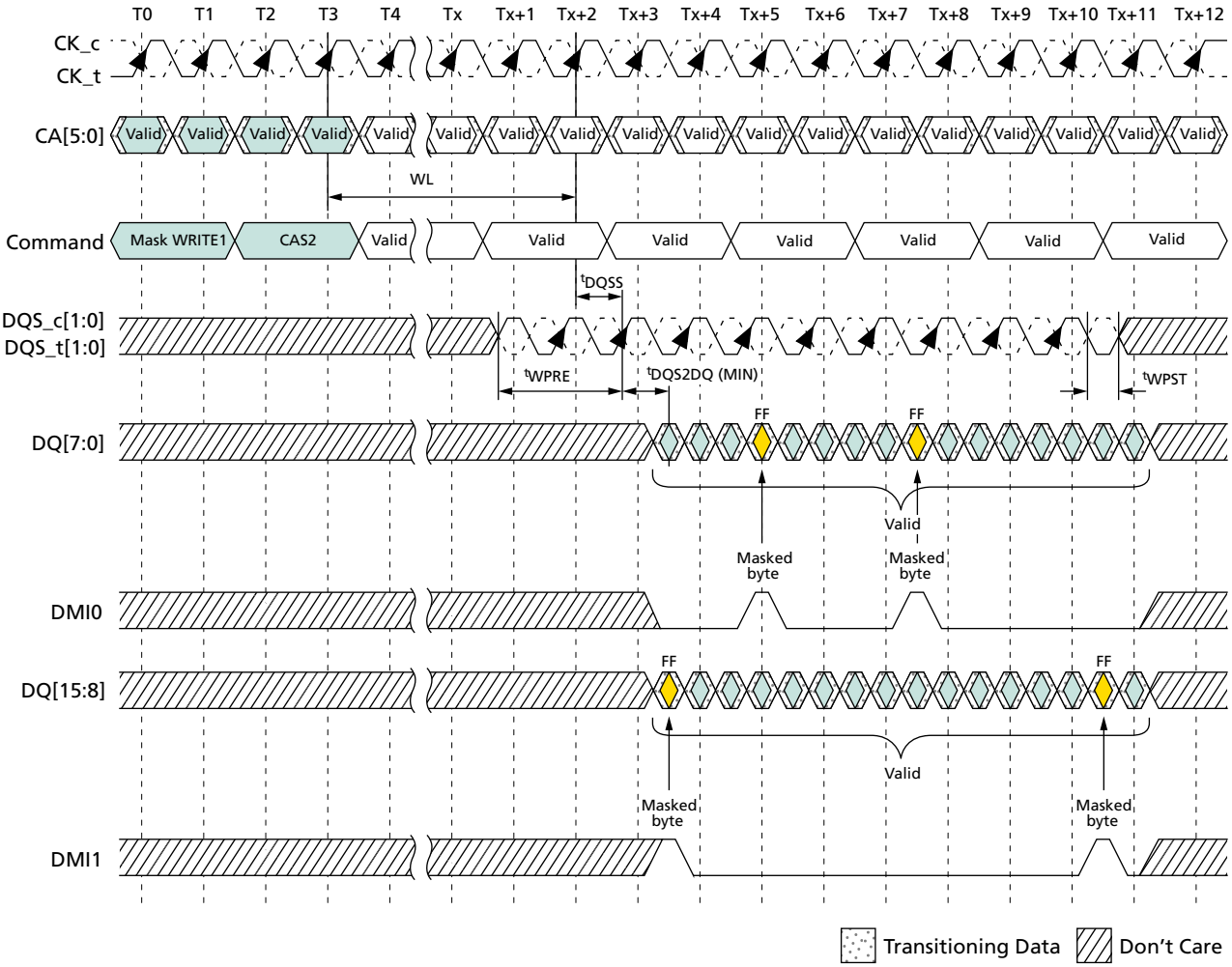
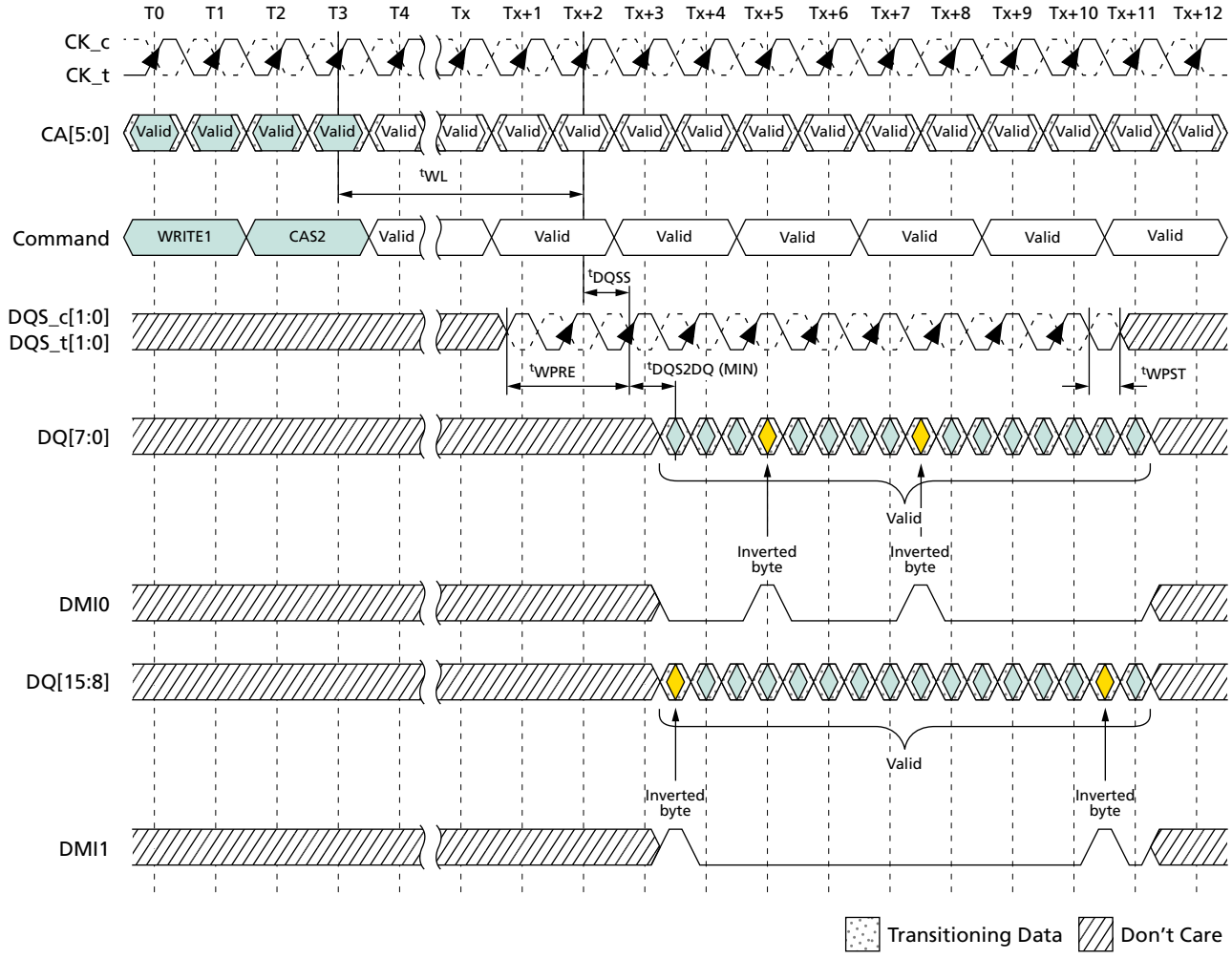


Figure 58: WRITE Command With DBI Enabled; DM Enabled: ^{t}WPRE = 2nCK and ^{t}WPST = 0.5nCK



Power-Down

Power-down is entered asynchronously when CKE is driven LOW and CS is LOW. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE, AUTO PRECHARGE, or REFRESH, are in progress, but the power-down I_{DD} specification will not be applied until such operations are complete.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure enough time to account for internal delay on the CKE signal path, DESELECT (DES) commands are required after CKE is driven LOW. This timing period is defined as ^{t}CKELCMD. CKE LOW will result in deactivation of input receivers after ^{t}CKCKEL has expired. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until ^{t}CKE,min is satisfied.

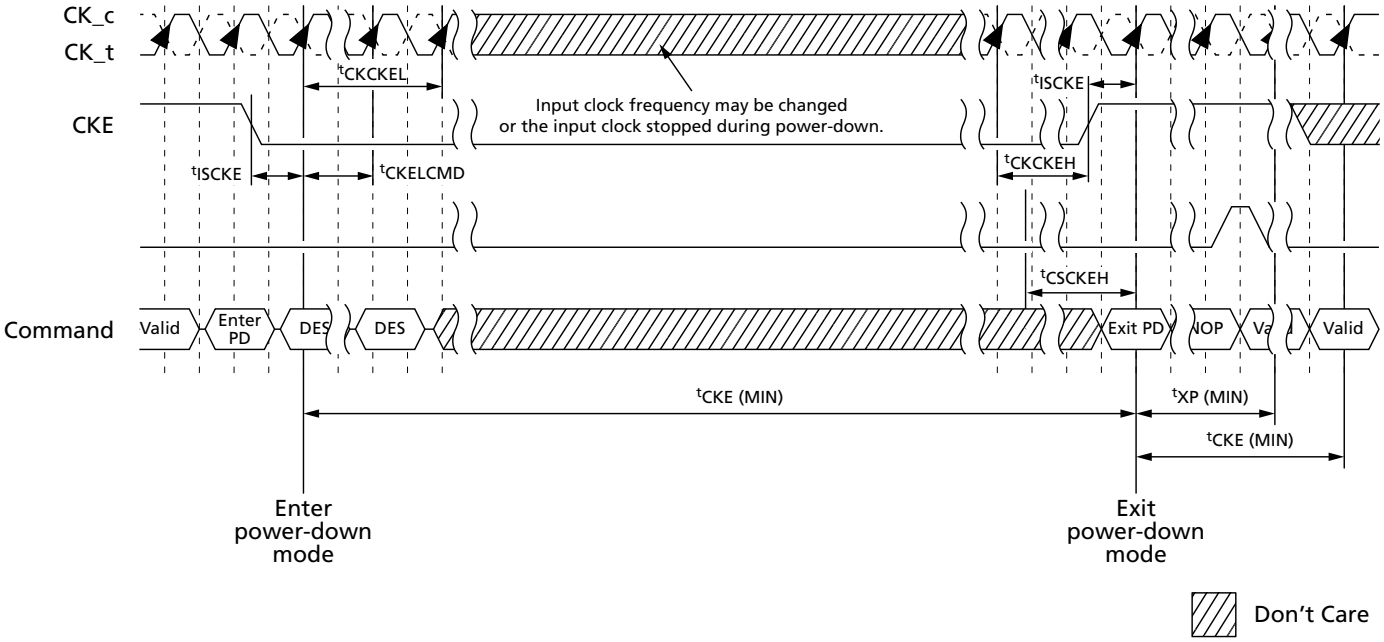
V_{DDQ} can be turned off during power-down. Prior to exiting power-down, V_{DDQ} must be within the respective minimum/maximum operating ranges.

No REFRESH operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in REFRESH Command.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS LOW in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until ^{t}CKE,min is satisfied. A valid, executable command can be applied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down EXIT latency is defined in the AC Timing table.

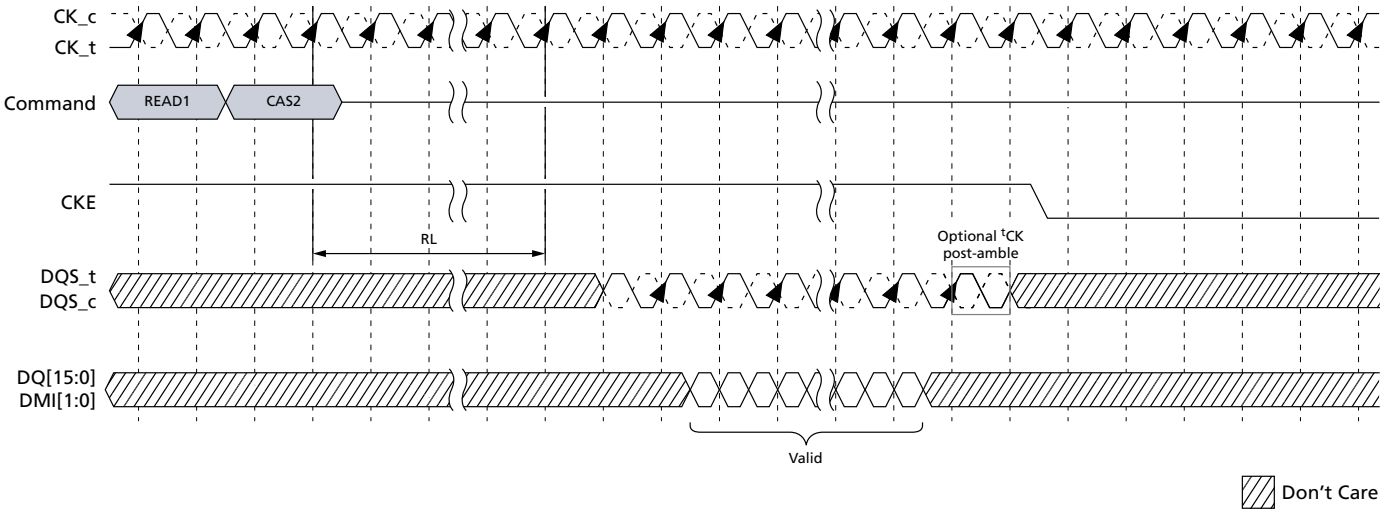
If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see On-Die Termination.

Figure 59: Power-Down Entry and Exit



Note: 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of RU(^{t}CKCKEH/^{t}CK) of stable clock prior to power-down exit, and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

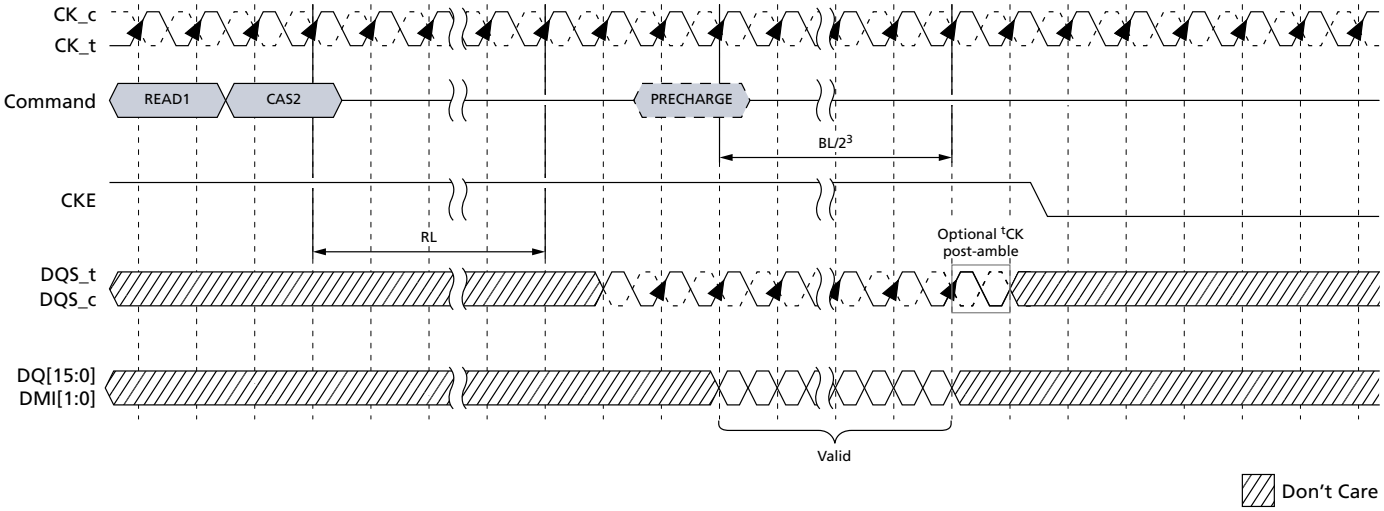
Figure 60: READ to Power-Down Entry



Notes: 1. CKE must be held HIGH until the end of the burst operation.
2. If optional ^{t}CK postamble is disabled, CKE can be driven LOW at RL × ^{t}CK + ^{t}DQSCK,max + BL/2 × ^{t}CK + 1 × ^{t}CK after the clock on which the CAS-2 command is registered. If optional ^{t}CK postamble is enabled, one additional clock cycle time is added.

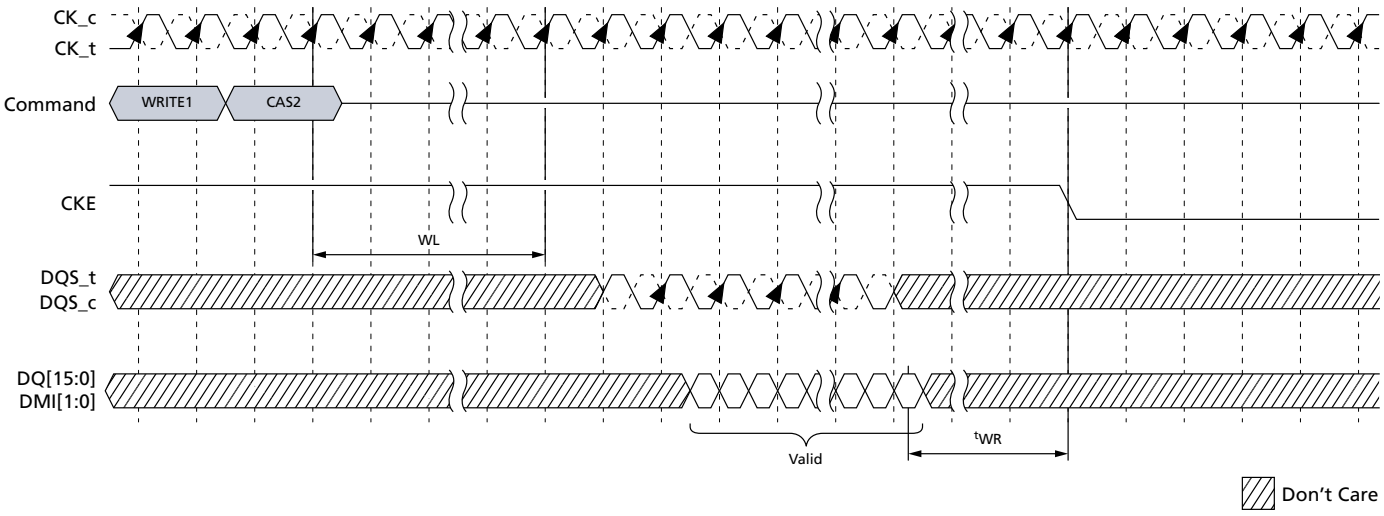
Proposal

Figure 61: READ with Auto Precharge to Power-Down Entry



Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. If optional ^{t}CK postamble is disabled, CKE can be driven LOW at RL × ^{t}CK + ^{t}DQSCK,max + BL/2 × ^{t}CK + 1 × ^{t}CK after the clock on which the CAS-2 command is registered. If optional ^{t}CK postamble is enabled, one additional clock cycle time is added.
3. BL/2 with ^{t}RTP = 7.5ns and ^{t}RAS,min must be satisfied.
4. Start of internal precharge.

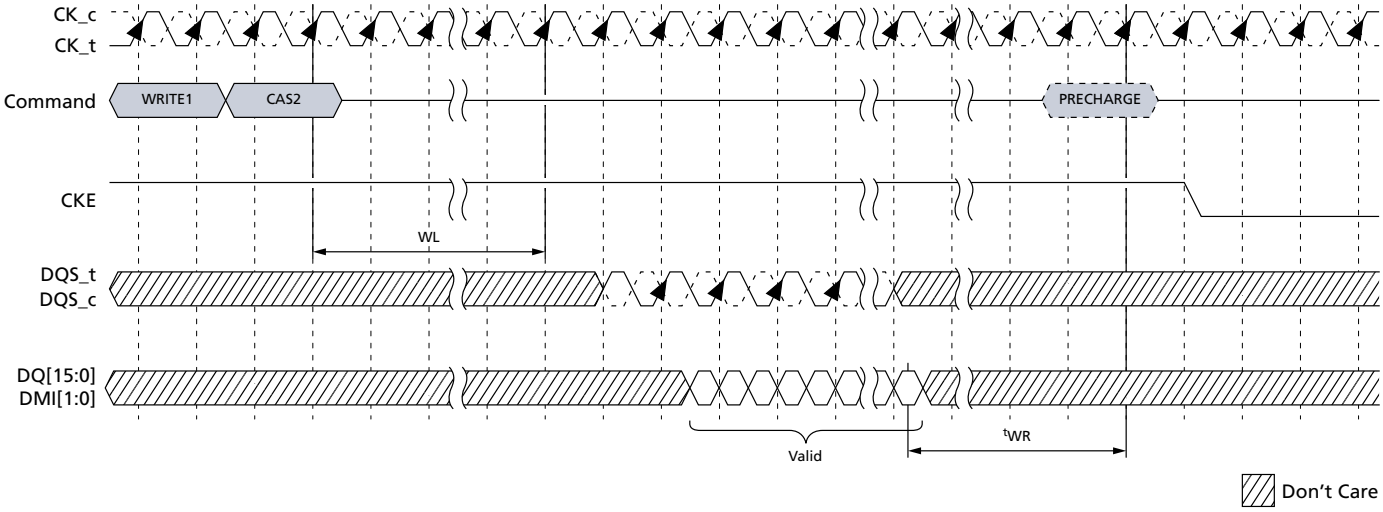
Figure 62: WRITE to Power-Down Entry



Note:
1. CKE can be driven LOW at WL × ^{t}CK + ^{t}DQSS + ^{t}DQS2DQ + BL/2 × ^{t}CK + ^{t}WR after the clock on which the CAS-2 command is registered.

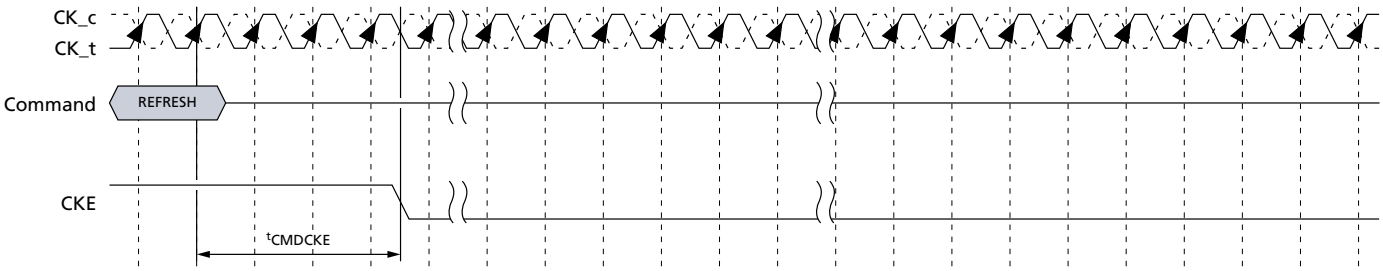
Proposal

Figure 63: Write with Auto Precharge to Power-Down Entry



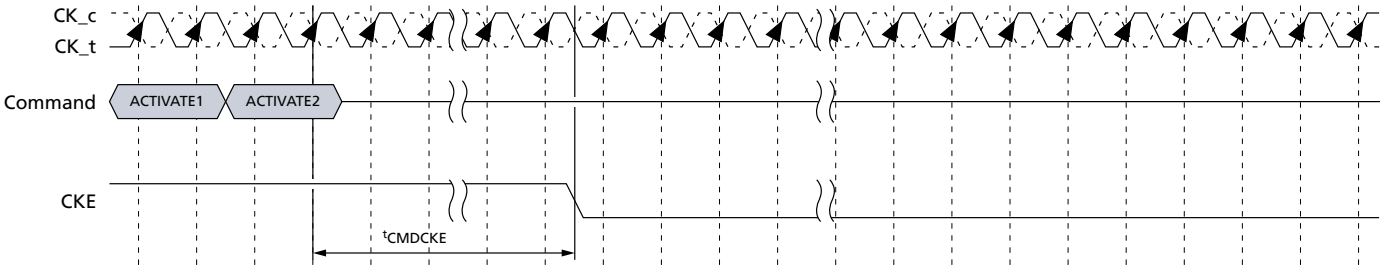
Note: 1. CKE can be driven LOW at WL × ^{t}CK + ^{t}DQSS + ^{t}DQS2DQ + BL/2 × ^{t}CK + ^{t}WR after the clock on which the CAS-2 command is registered.

Figure 64: Refresh Entry to Power-Down Entry



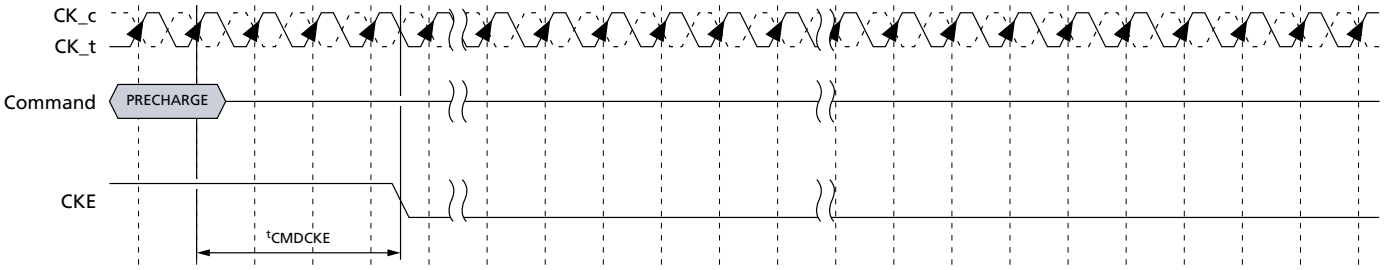
Note: 1. CKE can be driven LOW ^{t}CMDCKE after the clock on which the REFRESH command is registered.

Figure 65: ACTIVATE Command to Power-Down Entry



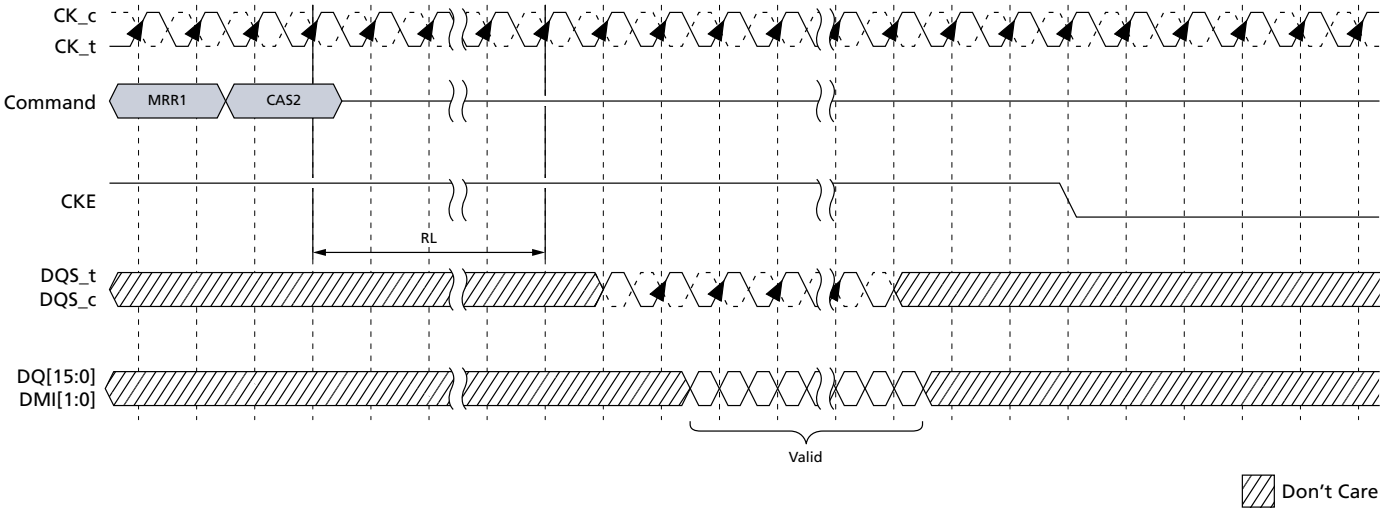
Note: 1. CKE can be driven LOW ^{t}CMDCKE after the clock on which the ACTIVATE-2 command is registered.

Figure 66: PRECHARGE Command to Power-Down Entry



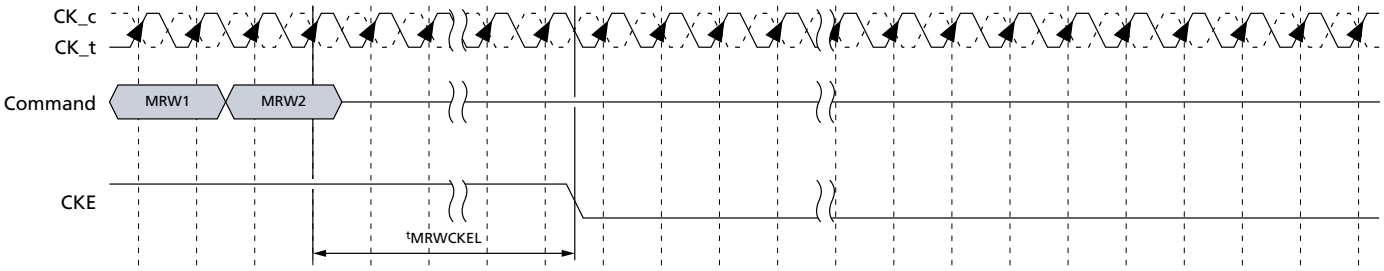
Note: 1. CKE can be driven LOW ^{t}CMDCKE after the clock on which the PRECHARGE command is registered.

Figure 67: MRR to Power-Down Entry



Notes: 1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be driven LOW at RL × ^{t}CK + ^{t}DQSCK,max + BL/2 × ^{t}CK + 1 × ^{t}CK after the clock on which the CAS-2 command is registered.

Figure 68: MRW to Power-Down Entry



Note: 1. CKE can be driven LOW ^{t}MRWCKEL after the clock on which the PRECHARGE command is registered.

Input Clock Stop and Frequency Change

Clock Frequency Change – CKE LOW

During CKE LOW, the device supports input clock frequency changes under the following conditions:

- ^{t}CK(abs) (MIN) is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, ^{t}RCD and ^{t}RP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of four clock cycles after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of two clock cycles prior to CKE going HIGH

After the input clock frequency changes and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, and so forth. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE LOW

During CKE LOW, the device supports clock stop under the following conditions:

- CK_t is held LOW and CK_c is held HIGH, or both are floated during clock stop
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to stopping the clock
- Related timing conditions, ^{t}RCD and ^{t}RP, have been met prior to stopping the clock
- The initial clock frequency must be maintained for a minimum of four clock cycles after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of two clock cycles prior to CKE going HIGH

Clock Frequency Change – CKE HIGH

During CKE HIGH, the device supports input clock frequency change under the following conditions:

- ^{t}CK(abs) (MIN) is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands (and any associated data bursts) have completed prior to changing the frequency
- Related timing conditions (^{t}RCD, ^{t}WR,^{t}WRA, ^{t}RP, ^{t}MRW, and ^{t}MRR) have been met prior to changing the frequency

- During clock frequency change, CS is held LOW
- The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of 2 × ^{t}CK + ^{t}XP

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, and so forth. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE HIGH

During CKE HIGH, the device supports clock stop under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop
- During clock stop, CS is held LOW
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands (and any associated data bursts) have completed prior to stopping the clock
- Related timing conditions (^{t}RCD, ^{t}WR,^{t}WRA, ^{t}RP, ^{t}MRW, and ^{t}MRR) have been met prior to stopping the clock
- The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of 2 × ^{t}CK + ^{t}XP

Frequency Set Points

Frequency set points enable the CA bus to be switched between two differing operating frequencies with changes in voltage swings and termination values, without ever being in an untrained state, which could result in a loss of communication to the device. This is accomplished by duplicating all CA bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency.

These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (frequency set point write/read) and the operating point controlled by MR bit FSP-OP (frequency set point operation). Changing the FSP-WR bit enables MR parameters to be changed for an alternate frequency set-point without affecting the current operation.

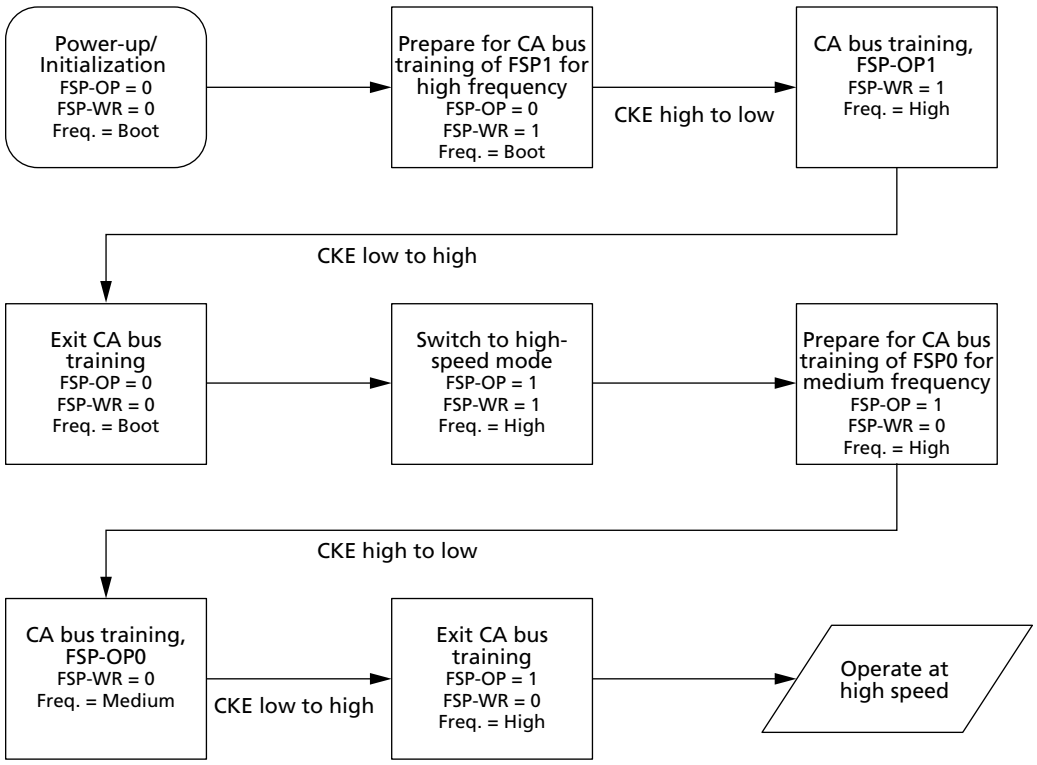
Once all necessary parameters have been written to the alternate set point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within ^{t}FC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include those listed below (see Mode Register Definition for more details):

- BL (burst length)
- WR-PRE (write preamble)
- RD-PRE (read preamble)
- nWR (write recovery for auto precharge)
- PST (postamble)
- RL (READ latency)
- WL (WRITE latency)
- WLS (WRITE latency set)
- PDDS (pull-down drive strength and R_x termination)
- DBI-RD (DBI-read enable)
- DBI-WR (DBI-write enable)
- DQ-ODT (DQ ODT value)
- CA-ODT (CA ODT value)
- VREF-CA ($V_{REF(CA)}$ value)
- VR-CA ($V_{REF(CA)}$ range)
- VREF-DQ ($V_{REF(DQ)}$ value)
- VR-DQ ($V_{REF(DQ)}$ range)
- SoC-ODT

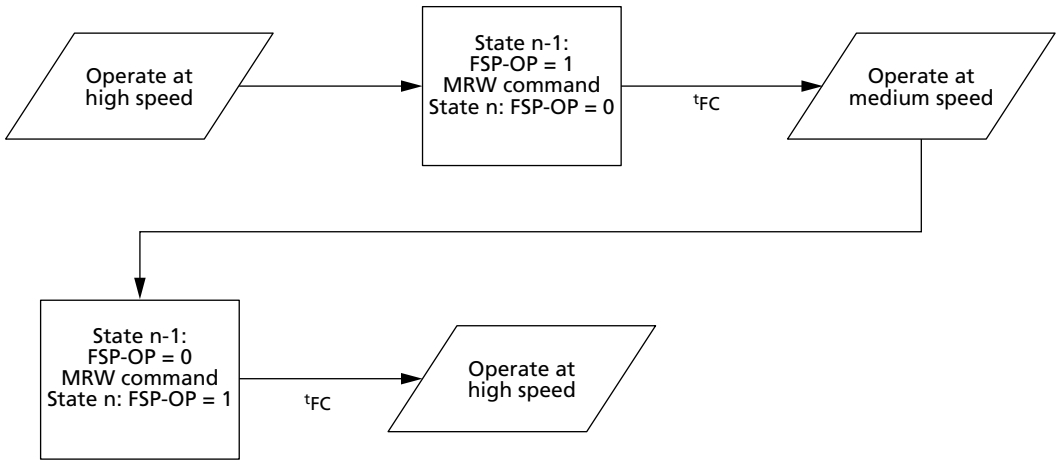
The device defaults to FSP-OP[0] at power-up. Both set points default to settings needed to operate in unterminated, low-frequency environments. To enable the device to operate at higher frequencies, a command bus training mode should be used to train the alternate frequency set point (see Command Bus Training for more details).

Figure 69: Example of Training for Two Frequency Set Points



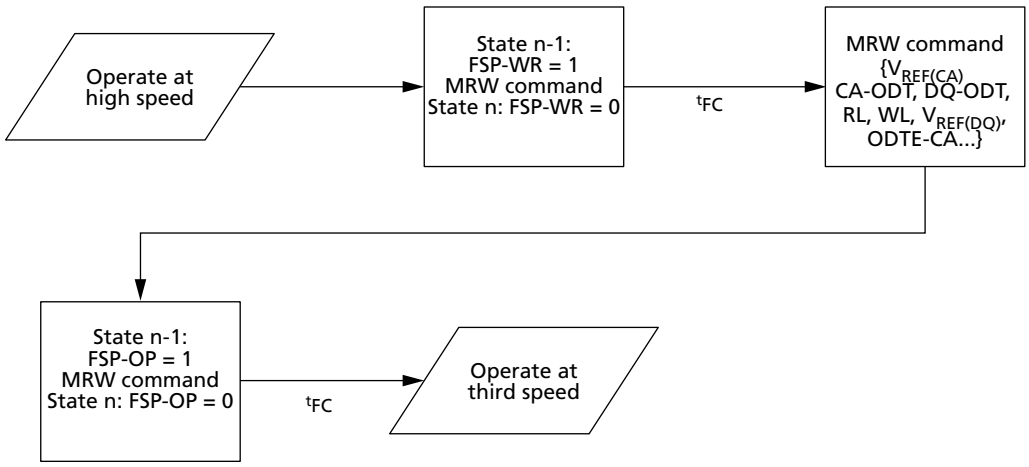
Once both of the frequency set points have been trained, switching between points can be performed with a single MRW followed by waiting for time ^{t}FC.

Figure 70: Example of Switching Between Two Trained Frequency Set Points



Switching to a third (or more) set point can be accomplished if the memory controller has stored the previously-trained values (in particular the $V_{REF(CA)}$ calibration value) and rewrites these to the alternate set point before switching FSP-OP.

Figure 71: Example of Switching to a Third Trained Frequency Set Point



Post-Package Repair

The device has an optional post-package repair (PPR) feature to provide an easy repair method once the device has been through final system assembly.

When supported, PPR enables a failed row address to be electrically repaired without removing the device from the system. With PPR, the device can correct one row per bank. Once programmed, the device cannot return to the preprogrammed state; thus, the controller should prevent unintended PPR entry and repair.

PPR support may be determined by MRR to MR0 OP[5] (= 1 if supported; = 0 if not supported).

Failed Row Address Repair

1. All banks must be precharged before entering PPR mode.
2. Enable PPR with MRW to OP[4] = 1, and wait ^{t}MRW.
3. Issue ACTIVATE (ACT-1 and ACT-2) commands with the address of the failed row.
4. Wait ^{t}PGM , then issue PRECHARGE(ab).
5. Wait ^{t}PGM_EXIT , allowing the DRAM to recognize the repaired row address.
6. Exit PPR mode with MRW to OP[4] = 0.
7. The device is ready for any valid command after ^{t}PGMPST.

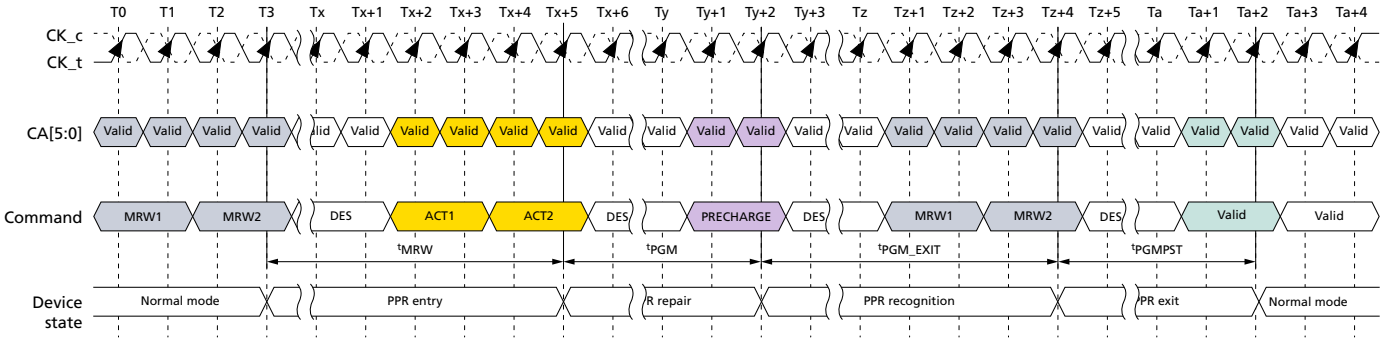
Once PPR mode is exited, the host can verify the repair by writing data into the target row and reading it back.

Proposal

Table 97: Post-Package Repair Timing Parameters

Parameter	Symbol	Min	Max	Units
PPR entry time	^{t}MRW	MAX (10ns, 10nCK)	–	ns
PPR programming time	^{t}PGM	200	250	ms
PPR exit time	^{t}PGM_EXIT	15	–	ns
New address setting time	^{t}PGMPST	50	–	us

Figure 72: Post-Package Repair



Notes:
1. CKE must remain HIGH with CK running (>10 MHz) during PPR mode.
2. Only specified commands or deselect are allowed after entering PPR mode.

Target Row Refresh

The device limits the number of times that a given row can be accessed within a refresh period, and is defined by the maximum activate count (MAC). After the MAC limit is reached, the adjacent rows must be refreshed to avoid data corruption. The target row (TRn) is the row that reached the MAC limit, and the adjacent rows are "victims." When the MAC limit is reached, the device should either receive all (R × 2) REFRESH commands before another row is activated, or the device should be placed into target row refresh (TRR) mode. The TRR mode is designed to refresh the victim rows adjacent to the TRn row that encountered the MAC limit.

A victim row can contain two TRn aggressor rows, one on either side. The cumulative value of the ACTIVATES operations from the two target rows on a victim row (within a bank) should not exceed the MAC value.

The TRR mode is entered via a MRW to MR4 OP[3] = 1, and is exited by completing the TRR sequence, which resets OP[3] = 0. The TRR mode may be interrupted and reissued by writing OP[3] = 0. If the TRR is interrupted before completion, the TRR must be cleared by issuing three PREpb commands to the target bank with ^{t}RP time between each command. By interrupting TRR, the victim row refresh is aborted and TRR must be reinitiated before issuing any new ACTIVATE commands.

Target Row Refresh Mode

The following steps must be performed when TRR mode is enabled. This mode requires three ACTIVATE and three PRECHARGE commands to complete. PREall or PREpb commands may be used interchangeably.

Prior to entering TRR mode, the device should be in an idle state. After setting MR4 OP[3] = 1, no commands are allowed until ^{t}MRD has been satisfied. While in TRR mode, only ACT and PRE commands are allowed until TRR is complete and the mode is exited.

The procedure to complete TRR is as follows:

- ACT-1/ACT-2 should be issued to the targeted bank/row followed 1.5 × ^{t}RAS later by PREpb (or PREall), then wait ^{t}RP.
- ACT-1/ACT-2 should again be issued to the targeted bank/row followed ^{t}RAS later by PREpb (or PREall), then wait ^{t}RP.
- ACT-1/ACT-2 should be issued a third time to the targeted bank/row followed t_{RAS} later by PREpb (or PREall), then wait $t_{RP} + t_{MRD}$.
- The TRR mode is automatically exited after the third cycle, and the SDRAM is now ready for any valid command.

Figure 73: Target Row Refresh Timing – TBD

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 98: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.6	V	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	–0.4	1.6	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.6	V	
Storage temperature	T_{STG}	–55	125	°C	2

Notes:
1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input/Output Capacitance

Table 99: Input/Output Capacitance

Parameter	Symbol	3200 MT/s		4267 MT/s		Unit	Notes
		Min	Max	Min	Max		
Input capacitance, CK_t and CK_c	C_{CK}	0.5	0.9	TBD	TBD	pF	
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.09	TBD	TBD		4
Input capacitance, all other input-only pins	C_I	0.5	0.9	TBD	TBD		5
Input capacitance delta, all other input-only pins	C_{DI}	–0.1	0.1	TBD	TBD		6
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C_{IO}	0.7	1.3	TBD	TBD		7,8
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.1	TBD	TBD		8,9
Input/output capacitance delta, DQ, DMI	C_{DIO}	–0.1	0.1	TBD	TBD		8,10
Input/output capacitance, ZQ pin	C_{ZQ}	0	2.0	TBD	TBD		

Notes:
1. Notes 1 and 2 apply to entire table
2. This parameter applies to LPDDR4 die only (does not include package capacitance).
3. This parameter is not subject to production testing; it is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, and V_{SS} applied; all other pins are left floating.

4. Absolute value of $CK_{CK\_t} - CK_{CK\_c}$.
5. C_I applies to CS, CKE, RESET_n, and CA[5:0].
6. $C_{DI} = C_I - 0.5 \times (C_{CK\_t} + CK_{CK\_c})$; it does not apply to CKE, RESET_n, or ODT(ca).
7. DMI loading matches DQ and DQS.
8. MR3 I/O configuration for pull-up/pull-down drive strength OP[5:0] = 000000b ($R_{ZQ}/7$).
9. Absolute value of C_{DQS_t} and C_{DQS_c}.
10. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS\_t} + C_{DQS\_c})$ in byte-lane.

Electrical Specifications – I_{DD} Specifications and Conditions

TBD

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 100: Recommended DC Operating Conditions

Symbol	LPDDR4-A			DRAM	Unit	Notes
	Min	Typ	Max			
V_{DD1}	1.7	1.8	1.95	Core 1 power	V	1, 2
V_{DD2}	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1, 2
V_{DDQ}	1.06	1.1	1.17	I/O buffer power	V	2, 3

Notes:
1. V_{DD1} uses significantly less power than V_{DD2}.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 100 MHz at the DRAM package ball.
3. The voltage noise tolerance from 250 KHz to 20 MHz must not exceed a pk-pk tolerance of 5% at the DRAM package ball.

Table 101: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	I_L	–2	2	µA	1

Notes:
1. Applies to CKE and RESET and CA, CS, CK_t, and CK_c with termination disabled. The input under test should be in the range $0V \le V_{IN} \le V_{DDQ}$. All other pins not under test = V_{SS}.
2. The DMI pin leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

Table 102: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	–25	85	°C
Elevated		85	105	°C

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. When using the device in the elevated temperature range, some derating may be required. See Mode Registers for vendor-specific derating.
3. Either the device case temperature rating or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the standard or elevated temperature range. For example, T_{CASE} could be above +85°C when the temperature sensor indicates a temperature of less than +85°C.

AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

TBD

VREF Tolerances

TBD

Input Signal

TBD

AC and DC Logic Input Levels for Differential Signals

TBD

Differential Input Cross Power Voltage

TBD

Slew Rate for Single-Ended Input Signals

TBD

Slew Rate for Differential Input Signals

TBD

AC and DC Output Measurement Levels

Table 103: Single-Ended AC and DC Output Levels – ODT Enabled

V_{OH} Level	Rx Termination (Nom)	$V_{OH(DC)}$ Accuracy			Units
		Min	Typ	Max	
$V_{DDQ/3}$	$R_{ZQ}/1$ (240Ω)	0.9	1.0	1.1	V_{OH}
	$R_{ZQ}/2$ (120Ω)				
	$R_{ZQ}/3$ (80Ω)				
	$R_{ZQ}/4$ (60Ω)				
	$R_{ZQ}/5$ (48Ω)				
	$R_{ZQ}/6$ (40Ω)				
$V_{DDQ/2.5}$	$R_{ZQ}/1$ (240Ω)	0.85	1.0	1.15	
	$R_{ZQ}/2$ (120Ω)				
	$R_{ZQ}/3$ (80Ω)				

Notes:
1. V_{OH} is the calibration comparison point. The output driver calibrates to the V_{OH} level ±10%.
2. Rx termination values must be set using the MRW command before ZQCal.
3. ZQCal is valid for any Rx termination value given the same V_{OH} level. If the V_{OH} level is changed, ZQCal must be retrained.

Single-Ended Output Slew Rate

TBD

Differential Output Slew Rate

TBD

Overshoot and Undershoot Specifications

TBD

Output Buffer Characteristics

Figure 74: LVSTL_11 Driver Output Timing Reference

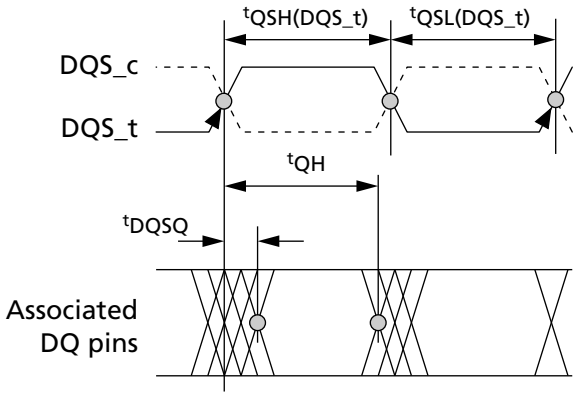
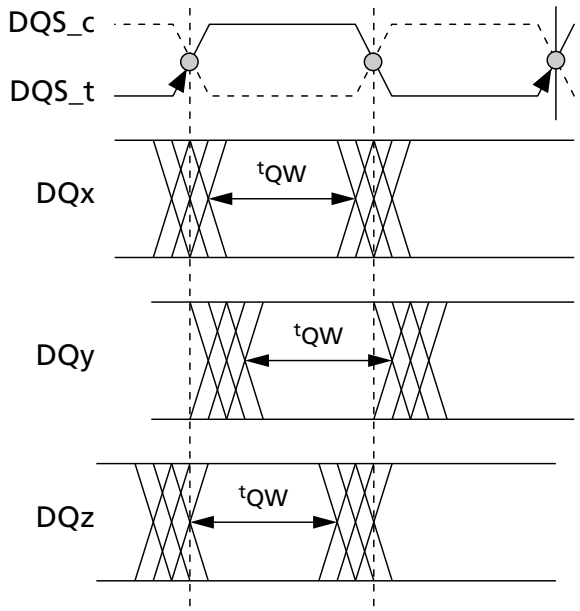


Figure 75: Read Data Timing Reference – Data Valid Windows



Driver Pull-up and Pull-Down Definition

TBD

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 104: Definitions and Calculations

Symbol	Description	Calculation	Notes
^{t}CK(avg) and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit ^{t}CK(avg) represents the actual clock average ^{t}CK(avg) of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. ^{t}CK(avg) can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t_{CK(avg)} = \left(\sum_{j=1}^{N} t_{CK_j}\right)/N$ Where N = 200	
^{t}CK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
^{t}CH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left(\sum_{j=1}^{N} t_{CH_j}\right)/(N \times t_{CK(avg)})$ Where N = 200	
^{t}CL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left(\sum_{j=1}^{N} t_{CL_j}\right)/(N \times t_{CK(avg)})$ Where N = 200	
^{t}JIT(per)	The single-period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).	$t_{JIT(per)} = \text{min/max of } \left(t_{CK_i} - t_{CK(avg)}\right)$ Where i = 1 to 200	1
^{t}JIT(per),act	The actual clock jitter for a given system.		
^{t}JIT(per), allowed	The specified clock period jitter allowance.		
^{t}JIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. ^{t}JIT(cc) defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \text{max of } \left(t_{CK_{i+1}} - t_{CK_i}\right)$	1
^{t}ERR(nper)	The cumulative error across *n* multiple consecutive cycles from ^{t}CK(avg).	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j}\right) - (n \times t_{CK(avg)})$	1
^{t}ERR(nper),act	The actual clock jitter over *n* cycles for a given system.		
^{t}ERR(nper), allowed	The specified clock jitter allowance over *n* cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	2

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Table 104: Definitions and Calculations (Continued)

Symbol	Description	Calculation	Notes
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	^{t}ERR(nper),max = (1 + 0.68LN(n)) × ^{t}JIT(per),max	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	^{t}JIT(duty),min = MIN((^{t}CH(abs),min – ^{t}CH(avg),min), (^{t}CL(abs),min – ^{t}CL(avg),min)) × ^{t}CK(avg) ^{t}JIT(duty),max = MAX((^{t}CH(abs),max – ^{t}CH(avg),max), (^{t}CL(abs),max – ^{t}CL(avg),max)) × ^{t}CK(avg)	

Notes: 1. Not subject to production testing.
2. Using these equations, ^{t}ERR(nper) tables can be generated for each ^{t}JIT(per),act value.

^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 105: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)

Notes: 1. ^{t}CK(avg),min is expressed in ps for this table.
2. ^{t}JIT(duty),min is a negative value.

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Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks, or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(^{t}nPARAM),act exceed ^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{nPARAM}} - {}^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cycle derating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceed the supported cumulative ^{t}ERR(^{t}nPARAM),allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^{t}CORE), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{CK(avg)}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (^{t}IS, ^{t}IH, ^{t}ISb, ^{t}IHb) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the ^{t}JIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

^{t}RPRE

When the device is operated with input clock jitter, ^{t}RPRE must be derated by the ^{t}JIT(per),act,max of the input clock that exceeds ^{t}JIT(per),allowed,max. Output deratings are relative to the input clock:

$$^{t}\text{RPRE(min,derated)} = 0.9 - \left(\frac{^{t}\text{JIT(per),act,max} - {}^{t}\text{JIT(per),allowed,max}}{^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR4 device has ^{t}CK(avg) = 625ps, ^{t}JIT(per),act,min = –xx, and ^{t}JIT(per),act,max = +xx ps, then ^{t}RPRE,min,derated = 0.9 - (^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) = 0.9 - (xx - xx)/xx = yy ^{t}CK(avg).

^{t}LZ(DQ), ^{t}HZ(DQ), ^{t}DQSCK, ^{t}LZ(DQS), ^{t}HZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where: *n* = 0,1; and *m* = 0–15, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by ^{t}JIT(per).

^{t}QSH, ^{t}QSL

These parameters are affected by duty cycle jitter, represented by ^{t}CH(abs)min and ^{t}CL(abs)min. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = MIN {(^{t}QSH(abs)min - ^{t}DQSQmax), (^{t}QSL(abs)min - DQSQmax)}. This minimum data valid window must be met at the target frequency regardless of clock jitter.

^{t}RPST

^{t}RPST is affected by duty cycle jitter, represented by ^{t}CL(abs). Therefore, ^{t}RPST(abs)min can be specified by ^{t}CL(abs)min. ^{t}RPST(abs)min = ^{t}CL(abs)min - 0.05 = ^{t}QSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

^{t}DS, ^{t}DH

These parameters are measured from a data signal (DMI*n or* DQ*m*, where *n* = 0, 1 and *m* = 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: *n* = 0,1) crossing. The specification values are not affected by the amount of ^{t}JIT(per) applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DSS, ^{t}DSH

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per)allowed}$.

^{t}DQSS

^{t}DQSS is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual ^{t}JIT(per),act of the input clock in excess of ^{t}JIT(per)allowed.

$$^{t}\text{DQSS(min,derated)} = 0.75 - \left(\frac{^{t}\text{JIT(per),act,min} - ^{t}\text{JIT(per),allowed, min}}{^{t}\text{CK(avg)}}\right)$$

$$^{t}\text{DQSS(max,derated)} = 1.25 - \left(\frac{^{t}\text{JIT(per),act,max} - ^{t}\text{JIT(per),allowed, max}}{^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into an LPDDR4 device has ^{t}CK(avg) = 625ps, ^{t}JIT(per),act,min = -xxps, and ^{t}JIT(per),act,max = +xx ps, then:

^{t}DQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx ^{t}CK(avg)

^{t}DQSS,(max,derated) = 1.25 - (xx – yy)/625 = xxxx ^{t}CK(avg)

Refresh Requirements

Table 106: Refresh Requirement Parameters (per density)

Parameter		Symbol	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	Unit
Density per channel		–	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	–
Number of banks		–	8					TBD	TBD	–
Refresh window (^{t}REFW):T_{CASE} ≤ 85°		^{t}REFW	32					TBD	TBD	ms
Refresh window (^{t}REFW): 1/2 rate refresh		^{t}REFW	16					TBD	TBD	ms
Refresh window (^{t}REFW): 1/4 rate refresh		^{t}REFW	8					TBD	TBD	ms
Required number of REFRESH commands in ^{t}REFW window		R	8192					TBD	TBD	–
Average refresh internal T_{CASE} ≤ 85°C	REFab	^{t}REFI	3.906					TBD	TBD	µs
	REFpb	^{t}REFIpb	488					TBD	TBD	ns
Average refresh internal (1/2 rate refresh)	REFab	^{t}REFI	1.953					TBD	TBD	µs
	REFpb	^{t}REFIpb	244					TBD	TBD	ns
Average refresh internal (1/4 rate refresh)	REFab	^{t}REFI	0.977					TBD	TBD	µs
	REFpb	^{t}REFIpb	122					TBD	TBD	ns
REFRESH cycle time (all banks)		^{t}RFCab	130	180		210		TBD	TBD	ns
REFRESH cycle time (per bank)		^{t}RFCpb	60	90		90		TBD	TBD	ns
Bytes refreshed per REF		–	16,384	24,576	32,768	49,152	65,536	TBD	TBD	–

Notes:
1. Refresh is defined with a 32ms window, which refreshes one half of the channel (or die). The entire channel (or die) is refreshed every 64ms.
2. Refresh for each channel is independent of the other channel or die, or other channels in a package. Power delivery in the system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

Table 107: READ and WRITE Latencies

Parameter	Value								Unit
Maximum clock frequency	266	533	800	1066	1333	1600	1867	2133	MHz
Maximum data rate	533	1066	1600	2133	2667	3200	3733	4267	MT/s
Average clock period	3759	1876	1250	938	750	625	536	469	ps
READ latency (DBI disabled)	6	10	14	20	24	28	32	36	^{t}CK(avg)
READ latency (DBI enabled)	6	12	16	22	28	32	36	40	
WRITE latency (Set A)	4	6	8	10	12	14	16	18	
WRITE latency (Set B)	4	8	12	18	22	26	30	34	

Preamble and Postamble

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via MODE REGISTER WRITE commands.

The read preamble is two ^{t}CK in length and is either static or has one clock toggle before the first latching edge. The read preamble option is enabled via MRW to MR1 OP[3] (0 = Static; 1 = Toggle).

The read postamble has a programmable option to extend the postamble by 1*n*CK (^{t}RPSTE). The extended postamble option is enabled via MRW to MR1 OP[7] (0 = 0.5*n*CK; 1 = 1.5*n*CK).

Figure 76: DQS Read Preamble/Postamble – Toggle Preamble

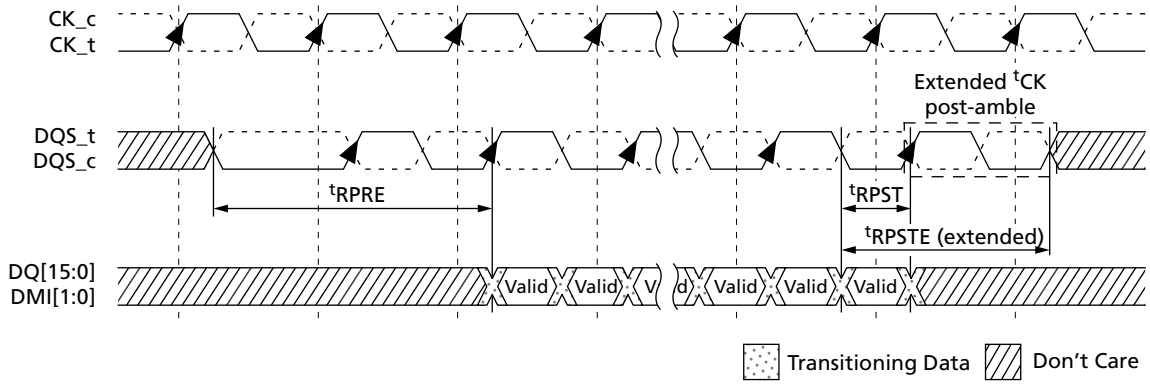


Figure 77: DQS Read Preamble/Postamble – Static Preamble

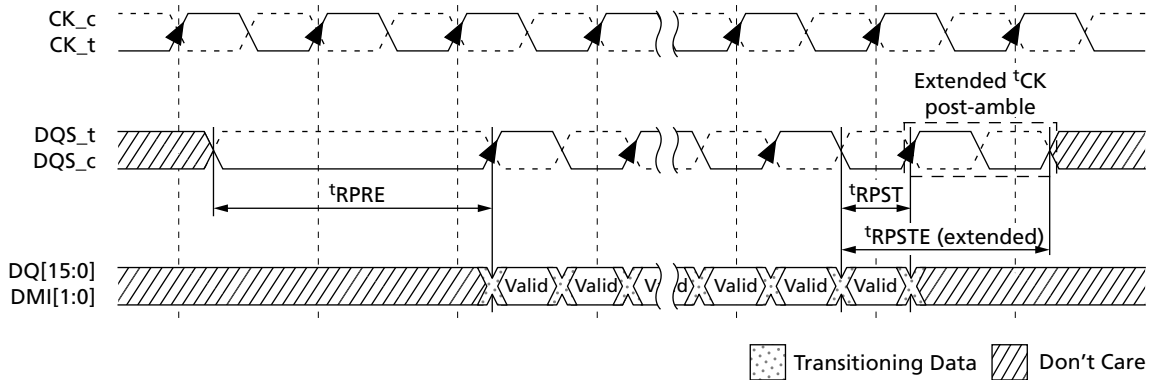


Figure 78: DQS Write Preamble/Postamble – CK ≤ TBD MHz

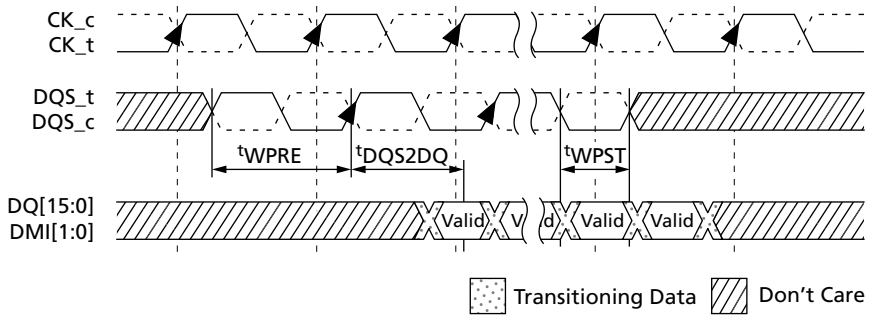
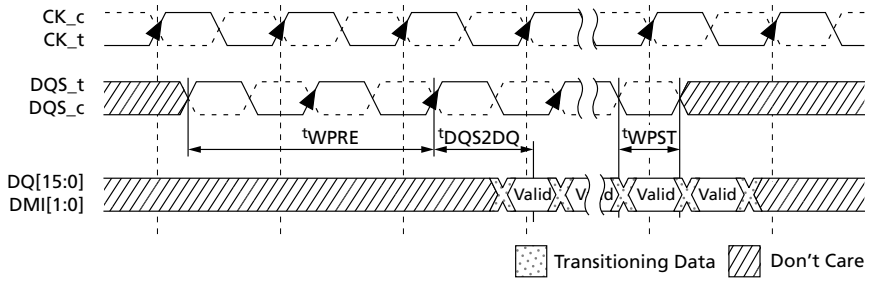


Figure 79: DQS Write Preamble/Postamble – CK > TBD MHz



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AC Timing

Table 108: Clock Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
Average clock period	^{t}CK(avg)	Min	3750	1875	1250	937	750	625	535	468	ps
		Max	100	100	100	100	100	100	100	100	ns
Average HIGH pulse width	^{t}CH(avg)	Min	0.46								^{t}CK(avg)
		Max	0.54								
Average LOW pulse width	^{t}CL(avg)	Min	0.46								^{t}CK(avg)
		Max	0.54								
Absolute clock period	^{t}CK(abs)	Min	^{t}CK(avg)min + ^{t}JIT(per)min								ps
Absolute clock HIGH pulse width	^{t}CH(abs)	Min	0.43								^{t}CK(avg)
		Max	0.57								
Absolute clock LOW pulse width	^{t}CL(abs)	Min	0.43								^{t}CK(avg)
		Max	0.57								
Clock period jitter	^{t}JIT(per)allowed	Min	TBD	TBD	TBD	TBD	TBD	–40	TBD	–20	ps
		Max	TBD	TBD	TBD	TBD	TBD	40	TBD	20	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	^{t}JIT(cc)allowed	Max	TBD	TBD	TBD	TBD	TBD	80	TBD	TBD	ps
Duty cycle jitter (with supported jitter)	^{t}JIT(duty)allowed	Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative errors across 2 cycles	^{t}ERR(2per)allowed	Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative errors across n cycles	^{t}ERR(nper)allowed	Min	^{t}ERR(nper)allowed,min = (1 + 0.68ln(n)) x ^{t}JIT(per)allowed,min								ps
		Max	^{t}ERR(nper)allowed,min = (1 + 0.68ln(n)) x ^{t}JIT(per)allowed,max								

Table 109: ZQ Calibration

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
ZQ calibration time	^{t}ZQCAL	Min	1								µs
ZQ calibration latch time	^{t}ZQLAT	Min	MAX(30ns,8nCK)								ns
ZQ calibration reset time	^{t}ZQRESET	Min	MAX(50ns,3nCK)								ns

Table 110: Read Output Timings

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS output access time from CK_t/CK_c	^{t}DQSCK	Min	1500								ps	
		Max	3500									
DQS output access time from CK_t/CK_c - voltage variation [1, 2, 3]	^{t}DQSCK_VOLT	Max	TBD								ps	
DQS output access time from CK_t/CK_c - temperature variation [1, 2, 3]	^{t}DQSCK_TEMP	Max	TBD								ps	
Data Timing												
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	^{t}DQSQ	Max	0.18	0.18	0.18	0.18	0.18	0.18	TBD	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	^{t}QH	Min	MIN(^{t}QSH, ^{t}QSL)								ps	1
Data output valid window time total, per pin (DBI-Disabled)	^{t}QW_total	Min	TBD								UI	1, 4
DQ output widow time deterministic, per pin (DBI-Disabled)	^{t}QW_dj		TBD								UI	1, 3, 4
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	^{t}DQSQ_DBI	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	^{t}QH_DBI	Min	TBD								ps	1
Data output valid window time total, per pin (DBI-Enabled)	^{t}QW_total_DBI	Min	TBD								UI	1, 4
Data Strobe Timing												
DQS_t, DQS_c differential output LOW time (DBI-Disabled)	^{t}QSL	Min	^{t}CL(abs) – TBD								^{t}CK(avg)	4, 5
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	^{t}QSH	Min	^{t}CH(abs) – TBD								^{t}CK(avg)	4, 6
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	^{t}QSL-DBI	Min	^{t}CL(abs) – TBD								^{t}CK(avg)	4, 5

Table 110: Read Output Timings (Continued)

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	tQSH-DBI	MIN	tCH(abs) – TBD								tCK(avg)	4, 6
Read preamble	tRPRE	Min	1.8								tCK(avg)	
Read postamble	tRPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(avg)	
DQS Low-Z from clock	tLZ(DQS)	Min	tDQSCK(min) – 300								ps	
DQ Low-Z from clock	tLZ(DQ)	Min	tDQSCK(min) – 300								ps	
DQS High-Z from clock	tHZ(DQS)	Min	tDQSCK(max) + 100								ps	
DQ High-Z from clock	tHZ(DQ)	Min	tDQSCK(max) + (1.4 x tDQSQ(max))								ps	

Notes:
1. DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER specification and measurement method are tbd.
2. The deterministic component of the total timing. Measurement method tbd.
3. This parameter will be characterized and guaranteed by design.
4. These values include input clock jitter assuming the min tCHabs(min) and tCLabs(min).
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
6. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.

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Table 111: Write Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
DQ and DMI data valid window (V_{IH} based)	tDIVW	Min	TBD	TBD	TBD	TBD	94	78	67	60	ps
DQ and DMI input pulse width	tDIPW	Min	0.45								UI
WRITE command to first DQS transition	tDQSS	Min	0.75								tCK(avg)
		Max	1.25								
DQS to DQ delay time	tDQS2DQ	Min	200								ps
		Max	800								
DQS input high-level width	tDQSH	–	TBD								tCK(avg)
DQS input low-level width	tDQSL	Min	TBD								tCK(avg)
DQS falling edge to CK set-up time	tDSS	Min	0.2								tCK(avg)
DQS falling edge from CK hold time	tDSH	Min	0.2								tCK(avg)
Write postamble	tWPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(avg)
Write preamble	tWPRE	Min	0.8		1.8						tCK(avg)

Table 112: CKE Input Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	max(5ns, 3nCK)								ns
Command path disable delay	tCPDED	Min	2								tCK(avg
Valid clock after CKE LOW	tCKCKEL	Min	max(7.5ns, 3 n CK)								ns
CK, CMD valid before CKE HIGH	tCKCKEH	Min	2								tCK(avg
		Max	–								
SREF-ENTRY command to CKE LOW	tESCKE	Min	2								tCK(avg
DESELECT command prior to CKE LOW	tCMDCKE	Min	2								tCK(avg
DESELECT command after CKE LOW	tCKELCMD	Min	max(7.5ns, 3nCK)								ns
DESELECT command prior to CKE HIGH	tCSCKEH	Min	TBD								ns
DESELECT command after CKE HIGH	tCKEHCMD	Min	max(7.5ns, 3nCK)								ns

Table 113: Command Address Input Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
Command/address valid window (referenced from CA V_{IL}/V_{IH} to CK V_{IX})	tCIVW	Min	0.3						TBD		tCK(avg)
Address and control input pulse width (referenced to V_{REF})	tIPW	Min	0.6						TBD		tCK(avg)

Table 114: Boot Parameters (10 MHz – 55 MHz)

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
Clock cycle time	tCKb	Min	TBD								ns
		Max	100								
DQS output data acess time from CK	tDQSCKb	Min	TBD								ns
		Max	10.0								
DQS edge to output data edge	tDQSQb	Max	1.2								ns

Table 115: Mode Register Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
MODE REGISTER WRITE (MRW) command period	tMRW	Min	max(10ns, 10nCK)								ns
MODE REGISTER READ (MRR) command period	tMRR	Min	8								tCK(avg)
Additional time after tXP has expired until the MRR command may be issued	tMRRI	Min	tRCDmin								ns

Table 116: Core Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
READ latency (DBI disabled)	RL-A	Min	6	10	14	20	24	28	32	36	tCK(avg)
WRITE latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	40	tCK(avg)
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	18	tCK(avg)
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	34	tCK(avg)
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab (with all-bank refresh) tRAS + tRPpb (with per-bank refresh)								ns
Minimum self refresh time (entry to exit)	tSR	Min	max(15ns, 3nCK)								ns
Self refresh exit to next valid command delay	tXSR	Min	max(tRFCab + 7.5ns, 2nCK)								ns
Exit power-down to next valid command delay	tXP	Min	max(7.5ns, 3nCK)								ns
CAS-to-CAS delay	tCCD	Min	8								tCK(avg)
CAS-to-CAS delay masked write	tCCDMW	MIN	32								tCK(avg)
INTERNAL READ to PRECHARGE command delay	tRTP	Min	max(7.5ns, 8nCK)								ns
RAS-to-CAS delay	tRCD	Min	max(18ns, 4nCK)								ns
Row precharge time (single bank)	tRPpb	Min	max(18ns, 3nCK)								ns
Row precharge time (all banks)	tRPab	Min	max(21ns, 3nCK)								ns
Row active time	tRAS	Min	max(42ns, 3nCK)								ns
		Min	35.1								µs
Write recovery time	tWR	Min	max(18ns, 4nCK)								ns
Write-to-read delay	tWTR	Min	max(10ns, 4nCK)								ns

Table 116: Core Parameters (Continued)

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
Active bank A to active bank B	^{t}RRD	Min	max(7.5ns, 2nCK)								ns
Precharge to precharge delay	^{t}PPD	Min	4								^{t}CK(avg)
Four-bank activate window	^{t}FAW	Min	40								ns

Table 117: CA Bus Training Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
CK, CMD valid after CKE LOW	^{t}CKELCK	Min	max(7.5ns, 3nCK)								^{t}CK(avg)
Data setup to DQS for V_{REF} latch	^{t}DStrain	Min	2								ns
Data Hold from DQS for V_{REF} latch	^{t}DHtrain	Min	2								ns
Data-out delay from CS/CA Input	^{t}ADR	Max	20								ns
CA BUS TRAINING command-to-command delay	^{t}CACD	Min	RU(^{t}ADR + 2nCK)								^{t}CK(avg)
CKE LOW to CS/CA input	^{t}CAENT	Min	10								ns
CA bus training CKE HIGH to DQ tri-state	^{t}MRZ	Min	1.5								ns
Mode Register Write Set Command Delay	^{t}MRD	Min	max(14ns, 10nCK)								ns
Vref Step Time – multiple steps	^{t}VREF_LONG	Max	200								ns
Vref Step Time – one step	^{t}VREF_SHORT	Max	80								ns

Proposal

Table 118: Write Leveling Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
DQS delay after write leveling mode entry	tWLDQSEN	Max	25								ns
First DQS edge after write leveling mode entry	tWLMRD	Min	40								ns
Write leveling output delay	tWLO	Max	20								ns
Write leveling hold time	tWLH	Min	135				TBD				ps
Write leveling setup time	tWLS	Min	135				TBD				ps
MODE REGISTER SET command delay for write leveling mode exit	tMRD	Min	max(14ns, 10nCK)								ns

Table 119: Temperature Derating Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
DQS output access time from CK (de-rated)	tDQSCKd	Max	TBD								ps
RAS-to-CAS delay (derated)	tRCDd	Min	TBD								ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	tRCd	Min	TBD								ns
ROW active time (derated)	tRASd	Min	TBD								ns
ROW precharge time (derated)	tRPd	Min	TBD								ns
Active bank-A to active bank-B (derated)	tRRD	Min	TBD								ns

Revision History

Rev. A – 9/2013

- Initial release